



SPECIFICATION FOR APPROVAL

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CRPS AC-DC 1600W

SWITCHING POWER SUPPLY

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W Manufacturer Part No.: KS260072

Customer Name _____

Customer Part NO. _____

Project Modify List

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SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



1. GENERAL	7
2. MECHANICAL OVERVIEW	7
2.1 DC output connector	8
2.2 Handle retention.....	9
2.3 Airflow Direction	9
2.4 LED indicator.....	9
2.5 Acoustic.....	9
3. AC INPUT REQUIREMENTS	10
3.1 AC inlet connector.....	10
3.2 Input voltage	10
3.3 Power factor and iTHD	10
3.4 AC line dropout / Holdup time / +12VSB Holdup time.....	11
3.5 EFFICIENCY	11
3.6 AC line fuse.....	11
3.7 AC inrush	12
3.8 AC line transient specification.....	12
3.9 Susceptibility requirements.....	13
3.10 Electrostatic Discharge Susceptibility.....	13
3.11 Fast transient/burst	13
3.12 Radiated immunity	13
3.13 Surge immunity	13
3.14 Voltage Interruptions	14
3.15 Power recovery.....	14
4. DC OUTPUT SPECIFICATION	14
4.1 Output Power / Currents	14
4.2 Voltage Regulation.....	14
4.3 Peak power	15
4.4 Dynamic Loading.....	15
4.5 Capacitive Loading	15
4.6 Grounding.....	15
4.7 Closed loop stability	16
4.8 Residual Voltage Immunity in Standby mode.....	16
4.9 Common Mode Noise	16
4.10 Soft Starting	16
4.11 Zero Load Stability Requirements	16

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



4.12	Hot Swap Requirements	16
4.13	Load Sharing	17
4.14	Ripple / Noise	17
4.15	Timing	17
4.16	PWOK Signal Timing Requirements	19
5.	PROTECTION CIRCUITS	20
5.1	Over Current Warning, Over Current Protection & Over Power Protection (OCW, OCP & OPP)	20
5.2	Fast Output Current sensing	21
5.3	Over Voltage Protection (OVP)	21
5.4	Over Temperature Protection (OTP)	21
6.	Control Signals	22
6.1	PS_ON# Input Signal (Pin A21)	22
6.2	PWOK (Power OK, Pin A25)	22
6.3	SMBAlert# (Pin A22)	23
6.4	RS- (Return Remote Sense, Pin A23)	23
6.5	RS+ (Main Output Remote Sense, Pin A24)	23
6.6	Cold Redundancy Bus (Pin B22, enable by system)	23
6.7	PRESENT_N# (Pin B24)	23
6.8	SDA (Pin A19)	24
6.9	SCL (Pin A20)	24
6.10	A0 (Pin B19)	24
6.11	A1 (Pin B20)	24
6.12	+12VLS (Pin B23)	24
7.	ENVIRONMENTAL REQUIREMENTS	25
7.1	Temperature	25
7.2	Humidity	25
7.3	Altitude	25
7.4	Mechanical shock	25
7.5	Random vibration	25
7.6	Thermal Shock (Shipping)	25
8.	FIRMWARE REQUIREMENTS	26
8.1	General Description	26
8.1.1	Scope	26
8.1.2	Reference Documents	26
8.1.3	Reference Information	26

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.1.3.1 Numerical Formats	26
8.1.3.2 Signal Names	26
8.1.3.3 Bit and Byte Order	26
8.1.4 Alert Response Address (ARA) Support.....	27
8.1.5 Abbreviations, Acronyms, and Definitions	27
8.1.6 Data Formats	27
8.1.6.1 Linear Data Format	27
8.1.6.1.1 Current, input voltage, power, temperature, fan speed, percentage and time duration.....	27
8.1.6.1.2 Output voltage related commands.....	28
8.1.7 Bus Speed	28
8.1.8 Device Base Addressing	28
8.2 Application Layer Requirements	28
8.2.2 PMBus Command List.....	30
8.2.3 Bits Filed Define.....	30
9.2.4 Reset of Status Bits	39
8.2.5 SMBALERT#.....	40
8.2.6 FRU Requirements.....	41
8.2.6.1 FRU Data	41
8.2.6.2 FRU Device Protocol	41
8.2.6.3 FRU Data Format	41
8.2.6.4 FRU Write Protection.....	42
8.3 CR & OFF Line Mode	42
8.3.1 Cold Redundancy Configuration	42
8.3.2 Power On/Off of Power Supplies in Cold Redundant Mode	43
8.4 Query(1Ah)	44
8.5 Black Box	46
8.5.1 When Data is saved to the Black Box	46
8.5.2 Black Box Events	46
8.5.3 Black Box Process	47
8.5.4 Commands.....	47
8.6 Firmware Update.....	49
8.6.1 FW Image Mapping.....	50
8.6.2 Summary of Commands and Capabilities Supported in Boot Loader Mode	50
8.6.3 Power Supply Operating Mode During and After Firmware Update Firmware update mode in OFF state with no power cycle needed:.....	50

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W Manufacturer Part No.: KS260072

- 8.6.4 Firmware Image Header..... 51
 - 8.6.5 PSU Upload Process..... 52
 - 8.6.6 PSU Flow During Powering ON 53
 - 8.6.7 Power Supply Commands..... 53
- 8.7 Filtering and Delay 56
 - 8.7.1 Filter processing..... 56
 - 8.7.2 Delay Processing..... 56
- 9. RELIABILITY 57
 - 9.1 Component De-rating 57
 - 9.2 Electrolytic Capacitor Life Requirement 57
 - 9.3 Fans..... 57
 - 9.4 Mean Time Between Failures (MTBF) 57
- 10. PRODUCT SAFETY AND EMC COMPLIANCE..... 57
 - 10.1 Product Safety Compliance..... 57
 - 10.2 Product EMC Compliance 57
 - 10.3 Dielectric Withstand (Hi-pot)..... 58
 - 10.4 Leakage (Touch) Current 58
- 11. NAME PLATE 59
- 12. PACKING (UNIT: MM) 60

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

1. GENERAL

This specification defines the functional requirements of the switching power supply. It is a redundant server power supply with features support hot plug N+M (N=2 max, M=2 max), dual outputs (+12Vand +12VSB), AC input auto ranging with power factor corrected, and internal fan(s) for force air cooling. Complies with Europe RoHS2.0 required.

2. MECHANICAL OVERVIEW

The physical size of the power supply is 40 (H) x 73.5 (W) x 185 (L) in milli-meter. The power supply contains asingle 40mm fan and incorporates a card edge output that interfaces with a 2x25 card edge connector in the system.The AC power cord plugs directly into the external face of the power supply.

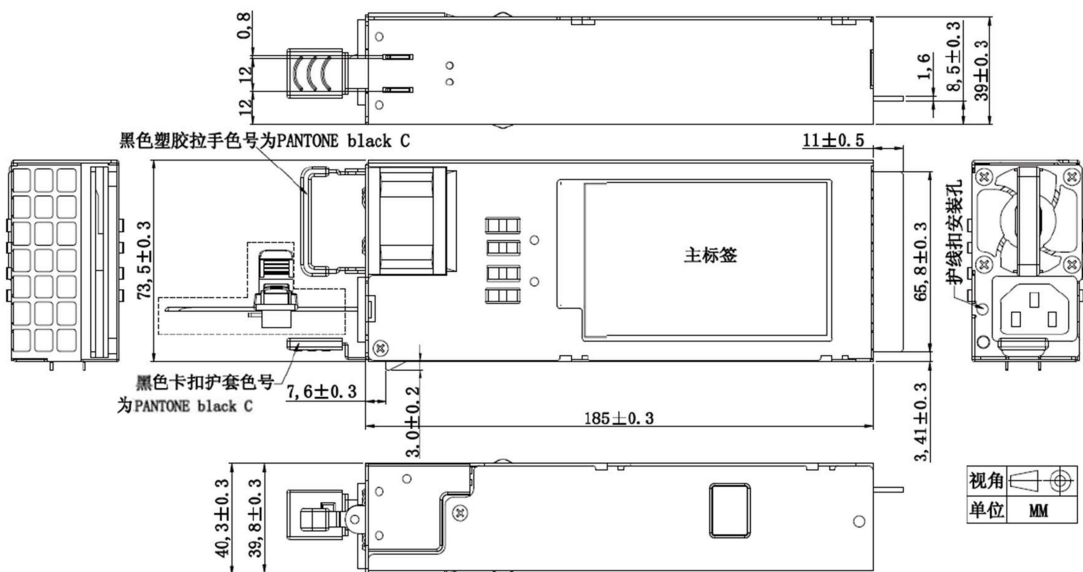


Figure 1 Shape

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



2.1 DC output connector

The power supply uses a card edge output connection for power and signal that is compatible with a 2x25Power Card Edge connector. Table 1 defines each output pin assignment on the output connector.

Table 1 Output Pin Assignment for 12Vout

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PS_ON#	B21	+12VSB
A22	SMBAlert#	B22	Cold Redundancy
A23	Return Remote Sense	B23	+12V load share bus
A24	+12V Remote Sense	B24	PRESENT_N#
A25	PWOK	B25	PSKILL#

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



2.2 Handle retention

The power supply has a handle to assist extraction. The module is able to be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord was plugged into the power supply.

2.3 Airflow Direction

The power supply is designed for supporting bi-airflow directions cooling purpose. The normal airflow means the air enters the PSU at DC output side and exits through the AC inlet side. The reverse airflow means the air enters the PSU at AC inlet side and exits through the DC output side.

2.4 LED indicator

The power supply uses a bi-color LED: Amber and Green to identify different operating states of the power supply. Table 2 defines the characteristics of the LED indicator.

Table 2 LED Characteristics

Power Supply Condition	LED State
Main output mode normal	Green
No AC power to power supplies	Off
PSU standby state AC present / PS off (+12VSB on or failure) or PSU in standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification.	1Hz Blink Green
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	Amber
Main output critical events causing a shutdown; Failure, OCP, Short Circuit, OVP, UVP, Fan Failure, OTP, Input OVP.	Amber
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow FAN	1Hz Blink Amber
Power supply FW updating mode	2Hz Blink Green

2.5 Acoustic

The power supply shall incorporate variable speed fan(s). Sound power must be measured according to ECMA 74 (www.ecma-international.org) and reported according to ISO 7779.

Table 3 PSU Sound Power Level

Load (%)	Temperature (°C)	Typical (dBA)
Full Output Rated Load	25	TBD
	35	TBD
	50	TBD
Half Output Rated Load	25	TBD
	35	TBD
	50	TBD
Note: Test with system fixture		

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



3. AC INPUT REQUIREMENTS

3.1 AC inlet connector

The AC input connector shall be an IEC 60320 C-14 power inlet. C-14 is rated for 10A / 250Vac.

3.2 Input voltage

The power supply must operate within all specified limits over the range shown in Table 6. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. The application of an input voltage below the minimum specified in Table 6 shall not cause damage to the power supply, including fuse failure.

Table 6 AC/DC Input Operation Rating

AC Line Input	Min.	Rated	Max.
Voltage Low Line (Vac)	90	100-127	140
Voltage High Line (Vac)	180	200-240	264
Frequency (Hz)	47	50/60	63

The steady state input current at 110 VAC input voltage and 1000 Watts shall not exceed 10 Amps. The steady state input current at 240 VAC input voltage and 1600 Watts shall not exceed 10 Amps. Note: The brown in/out testing shall not exceed low line max load.

3.3 Power factor and iTHD

The power supply must meet the power factor and current iTHD requirements that within Energy Star® Program Requirements for Computer Servers.

Table 4 Power Factor Requirements

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.90	> 0.96	> 0.98	> 0.99
Input conditions	200Vac to 240Vac, 50Hz/60Hz.			

Table 5 iTHD Requirements

Output power	> 5% & ≤ 10%	> 10% & < 20%	≥ 20%	≥ 40%	≥ 50%
Max. iTHD (%)	≤ 20%	≤ 15%	≤ 12%	≤ 8%	≤ 6%
Input conditions	200Vac to 240Vac and 50/60Hz				

Tested according to Generalized Internal Power Supply Efficiency Testing Protocol Rev6.7. This is posted at <https://plugloadsolutions.com/80pluspowersupplies.aspx>.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

3.4 AC line dropout / Holdup time / +12VSB Holdup time

An AC line dropout is defined to be when the rated AC input drops to 0Vac at any phase of the AC line for anylength of time. During an AC dropout the power supply shall meet the output voltage regulation limits. If the ACdropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. Adropout of the AC line for any duration shall not cause damage to the power supply.

AC line +12VSB Holdup time

The +12VSB output voltage shall stay in regulation under its full load (static or dynamic) during an AC dropout duration up to 70msec whether the power supply is in ON or OFF state (PS_ON# asserted or de-asserted).

Table 7 AC Drop Out Specification

Load	ACdropout
0% to 70% of rated load	10ms

Note: This test condition loading is 100% of maxloading.

3.5 EFFICIENCY

The following table shows the minimum efficiency requirements according to the proportional loading methoddefined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7 at 230Vac/60Hzand 25°C conditions excluded the losses of PSU fan.

Table 11 PSU Efficiency

Efficiency	10% Load	20% Load	50% Load	100% Load
Platinum	82%	92%	94%	91%

3.6 AC line fuse

The power supply incorporates a fast blow type fuse at AC input side. AC inrush current and all protection circuits, including DC output overload or shorted output conditions, in the power supply shall not cause the AC line fuse to open under any condition. The fuse should be open prior to C63 Breaker once internal fail happen.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072



3.7 AC inrush

The cold start inrush current during 1~1150ms shall be less than 35A at 25°C/240V.

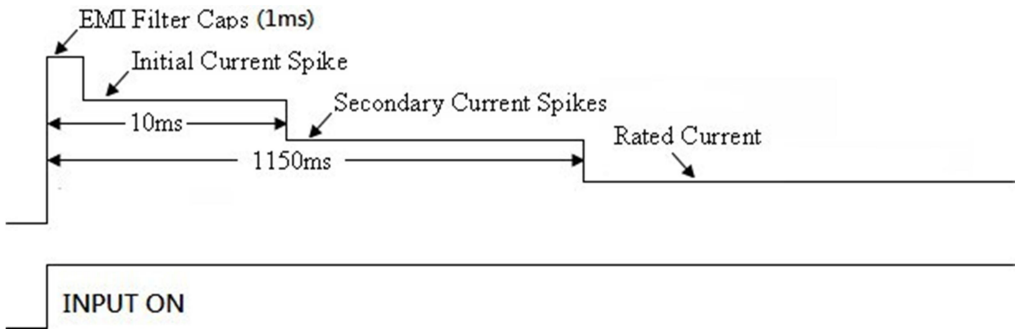


Figure 7

During a single cycle AC dropout condition or during repetitive ON/OFF cycling of AC, the warm start inrushcurrent must be less than 55A at 25°C/240V.

Note:

1. Due to line filter charging, the inrush current is ignored during 0~1msec after AC power turn on.
2. Peak inrush current at any allowable operating temperature shall not open line fuse/breaker, or cause damage to the power supply unit.

3.8 AC line transient specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” will be defined as the ACline voltage dropping below rated voltage conditions. “Surge” will be defined to refer to conditions when the ACline voltage rises above rated voltage.

Table 8 AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%	Rated AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Rated AC Voltage ranges	50/60Hz	Loss of function acceptable, self-recoverable

Table 9 AC Line Surge Transient Performance

AC Line Surge (10sec interval between each surging)				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Rated AC Voltages	50/60Hz	No loss of function or performance

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072



0 to 1/2 AC cycle	30%	Mid-level of rated AC Voltages	50/60Hz	No loss of function or performance
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3.9 Susceptibility requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an internal EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 10 Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended, No degradation of performance.
B	The apparatus shall continue to operate as intended, No degradation of performance beyond spec limits after the test.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.10 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55035:2017+A11:2020 and CISPR35: 2016 using the EN61000-4-2:2009 and IEC 61000-4-2: 2008 test standard and performance criteria B defined in Table 10.

3.11 Fast transient/burst

The power supply shall comply with the limits defined in EN 55035:2017+A11:2020 and CISPR35: 2016 using the EN61000-4-4: 2012 and IEC 61000-4-4: 2012 test standard and performance criteria B defined on Table 10.

3.12 Radiated immunity

The power supply shall comply with the limits defined in EN 55035:2017+A11:2020 and CISPR35: 2016 using the EN61000-4-3: 2006 +A1: 2008 +A2: 2010 and IEC 61000-4-3: 2006 _A1: 2007 +A2: 2010 test standard and performance criteria A defined on Table 10.

3.13 Surge immunity

The power supply shall comply with the limits defined in EN 55035:2017+A11:2020 and CISPR35: 2016 using the EN61000-4-5: 2014 and IEC 61000-4-5: 2014 test standard and performance criteria B defined on Table 10. The test condition: ±2kV/12ohm line to earth and ±1kV/2ohm line to line.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



3.14 Voltage Interruptions

The power supply shall comply with the limits defined in EN 55035:2017+A11:2020 and CISPR35: 2016 using the IEC61000-4-11: 2004 and IEC 61000-4-11: 2004 test standard and performance criteria C defined on Table 10.

3.15 Power recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

4. DC OUTPUT SPECIFICATION

4.1 Output Power / Currents

The following table defines the power supply output current rating. The power supply shall meet both static and dynamic voltage regulation limits for all conditions. No damaged shall be occurred under no load condition at all inputs defined in Table 12 and any operating ambient conditions.

Table 12 Output Current Rating

Input Range	Main Output	Min. Current	Max. Current
110VAC - 127VAC	+12V	1A	82A
200VAC - 240VAC	+12V	1A	132A
90VAC - 264VAC	+12VSB	0A	3.0A

4.2 Voltage Regulation

The power supply output voltages shall stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple & noise. These shall be measured at the output connectors.

Table 13 Voltage Regulation Limits

	VOLATGE REGULATION		
	Min	Typical	Max
+12V(Dynamic)	11.4V	12.0V	12.6V
+12V(Static)	11.4V		12.6V
+12VSB(Dynamic)	11.4V	12.0V	12.6V
+12VSB(Static)	11.4V		12.6V

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



4.3 Peak power

For peak loads above the Pmax.app peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 100µsec. For peak loads up to Pmax.app peak load level the PSU must not assert SMBAlert# if the peak load duration is <10msec. If the peak load last longer than 10msec the PSU may assert SMBAlert# to throttle the load within 15msec. Table 15 below are PSU requirements for Pmax peak load conditons.

Table 14 Peak Power Test Condition

Pmax Peak load	Peak current	System capacitance	SMBAlert# timing	Peak load duration	Voltage undershoot
Rated + 540W	Rated + 45A	6 x 1,500uF	< 20usec	100usec	-2%

4.4 Dynamic Loading

The output voltages shall remain within limits specified in Table 15 for the step loading and capacitive loading. The load transient repetition rate shall be tested between 50Hz and 10KHz at duty cycles ranging from 10% to 90%. The step load may occur anywhere within the MIN load to the Peak load conditions.

Table 15 Transient Load Requirements

Output	Δ Step Load Size (See note)	Load Slew Rate	Test capacitive Load
+12V	60% of max load	0.5 A/µsec	1,000 µF
+12VSB	1.0A	0.5 A/µsec	1,000 µF

Note: For dynamic condition +12V min loading is 1A

4.5 Capacitive Loading

The power supply shall be stable and meet all limits with the following capacitive loading ranges.

Table 16 Capacitive Loading Conditions

Output	MIN	MAX	Units
+12V	2200	20000	µF
+12VSB	100	3100	µF

Note: The minimum capacitive load on Main output is required to hold regulation during Cold Redundancy mode power supply failure and power supply hot swapping.

4.6 Grounding

The output ground (GND) pins of the power supply provide the output power return path. And all the GND pins are connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0m Ω . This path may be used to carry DC current.

4.7 Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 5.6. A minimum of: 45 degrees phase margin and -10dB gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

4.8 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PS0N# signal is de-asserted.

4.9 Common Mode Noise

The Common Mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz. The measurement shall be made across a 100 Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).

4.10 Soft Starting

The power supply contains a control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

4.11 Zero Load Stability Requirements

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

4.12 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply used a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



4.13 Load Sharing

Main output has active load sharing function by tying all the +12VLS together, to support active load sharing.

At N+M (N=2 max, M=2 max) redundant power supply system, Main outputs with active current sharing will share load

Current within 10% tolerance at each PSU has 10%~20% of its high line load and 5% tolerance at > 20% high line load.

Redundant backup one of the power failures cannot affect other power supply operations and outputs.

Table 17 Current Sharing Bus Requirements

Item	Description	Min.	Type	Max.	Unit
Vcs	Current sharing bus voltage under full load conditions	7.6	8	8.4	V
Vcs	Current sharing bus voltage under no-load conditions	0	0.125	0.175	V
Vcs/Iout	The current sharing bus climbs the slope, that is, the current sharing bus voltage at different output currents.	7.6/Irated	8/Irated	8.4/Irated	V/A

4.14 Ripple / Noise

The maximum ripple/noise output of the power supply is defined in Table 18.

This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors.

A proper polymer capacitor in parallel with a 0.1μF ceramic capacitor and 10μF ceramic capacitor is placed at the point of measurement. The length of twisted wire from connectors to probe should not longer than 50mm.

Table 18 Output Ripple and Noise

+12V	120mVpp
+12VSB	120mVpp

Note: The minimum load for the test condition on Main output rail shall be 1A; the minimum load for the test condition on +12VSB rail shall be 0.1A.

4.15 Timing

Figure 10 and Table 19 define the timing sequence for the power supply operation. Main output shall rise monotonically.

Table below shows the timing requirements for the power supply being turned on and off two different ways; 1) via the AC input with PSON held low; 2) via the PSON signal with the AC input applied.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

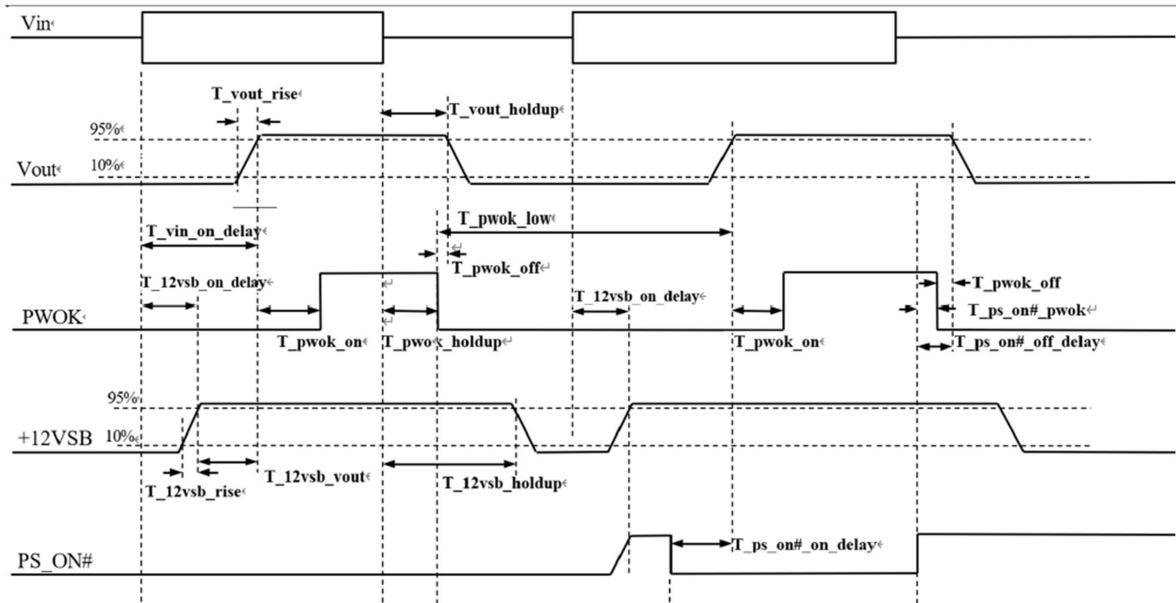


Figure 10 Turn On/Off Timing

Table 18 Power Supply Timing Requirements

Item	Description	MIN	MAX	UNIT
T_{vout_rise}	Output voltage rise time for Main output and +12VSB from 10% to within regulation limits.	5	70	ms
$T_{12vsb_on_delay}$	Delay from AC being applied to +12VSB being within regulation.		1500	ms
$T_{vin_on_delay}$	Delay from AC being applied to all output voltages being within regulation.		3000	ms
T_{vout_holdup}	Time Main output voltage stay within regulation after loss of AC, PSU works under 70% load.	11		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of $PWOK$, PSU works under 70% load.	10		ms
$T_{ps_on\#_off_delay}$	Delay from $PS_ON\#$ de-asserted to power supply turning off.		5	ms
$T_{ps_on\#_on_delay}$	Delay from $PS_ON\#$ active to output voltages within regulation limits.	5	400	ms
$T_{ps_on\#_pwok}$	Delay from $PS_ON\#$ deactivate to $PWOK$ being de-asserted.		5	ms
T_{pwok_on}	Delay from output voltages within regulation limits to $PWOK$ asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from $PWOK$ de-asserted to output voltages dropping out of regulation limits.	1	Configurable Via PMBu	ms
T_{pwok_low}	Duration of $PWOK$ being in the de-asserted state during an off/on cycle using AC or the $PS_ON\#$ signal.	100		ms
T_{12vsb_vout}	Delay from +12VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{12vsb_holdup}	Time the +12VSB output voltage stays within regulation after loss of AC.	70		ms

Note:

The test load for $T_{ps_on\#_off_delay}$ shall be 100% load.

The T_{pwok_holdup} and T_{pwok_off} times are the default values in the PUS when it is being energized; however, the system now can configure the warning time established by T_{pwok_off} to have a different value, refer to Section 5.16.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072



4.16 PWOK Signal Timing Requirements

The PWOK signal timing shall be as stated in Table 18. Timing requirements when the power supply is being energized (AC/DC is applied), however the warning time established by T_{pwok_off} shall be configurable via PMBus command MFR_PWOK_WARNING_TIME (F0h) using linear format it is recommended to use 1ms steps and the power supply shall guarantee at least the minimum warning time configured, it is recommended to have a jitter no more than 1.5ms. Figure 11 shows the timing diagram. T_{pwok_off} value shall return to default after an AC cycle only.

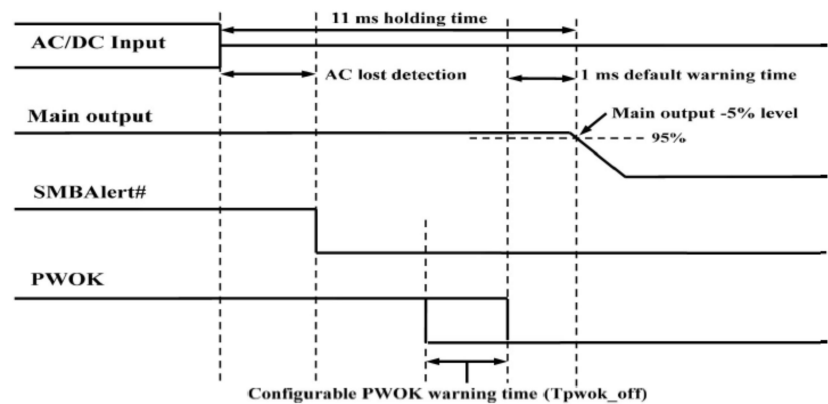


Figure 11

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



5. PROTECTION CIRCUITS

Protection circuits inside the power supply shall only cause the power supply's main outputs to shut down. The power supply will latch off after auto-recovering 3 times. The power supply latches off due to a protection circuit tripping, an AC cycle OFF for 1sec, a PSON# cycle HIGH for 1sec, operation command for 1sec shall be able to reset the power supply.

5.1 Over Current Warning, Over Current Protection & Over Power Protection (OCW, OCP & OPP)

The power supply shall have over current protection (OCP), over current warning (OCW), and over power protection (OPP) limits as defined in below table. These are defined to protect the PSU and to allow peak currents to power the system without PSU shutting down.

Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the PSU but also to allow peak current to the system without throttling the system.

When OCP trips, it shall shut down and latch OFF the PSU. This latch shall be cleared by toggling the PS_ON# signal or by an AC power interruption (Except the +12VSB protection occurred). The power supply shall not be damaged from repeated power cycling on this condition. +12VSB will be auto-recovered after removing OCP limit.

Table 19 Output Protection Table

Input	Parameter	Min	Nominal	Max	Uni	SMBAlert# delay	Fault delay
Low Line 90VAC - 140VAC Pout=1000W Iout=87A	OCW	105%	-	-	A	>60ms	>20s
	OCP	110%	-	-		>60ms	>100ms
	SCP	>150%				Immediate	Immediate
	OPW			OPP-50W	W	>3s	NA
	OPP	-		1350		>3ms	>5ms
High Line 180VAC - 264VAC Pout=1600W Iout=137A	OCW	110%	-	-	A	>60ms	>20s
	OCP1	120%	-	-		>60ms	>11s
	OCP2	140%				>60ms	>100ms
	SCP	>170%			W	Immediate	Immediate
	OPW			OPP-50W		>3s	NA
	OPP			2400		>3ms	>5ms
90 VAC -264VAC	12VSB OCP	3.5	4	4.5	A	NA	NA

Note:

1. OCW must occurred before the OPP & OCP.
2. PSU can trigger OTP during overload condition.
3. The output rating please refer to Table 12

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



5.2 Fast Output Current sensing

The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the over power protection threshold in the PSU. The SMBAlert# signal must always assert before the over power protection threshold is exceeded. The requirements are stated in Table 19.

5.3 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. Main output shall shutdown and latch off the PSU after auto-recovering 3 times when an over voltage condition occurs. This latch shall be cleared by toggling the PS_ON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels defined in Table 21 when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. +12VSB will be auto-recovered after removing OVP limit.

Table 21 Over Voltage Protection (OVP) Limits

	Minimum	Maximum
+12V over voltage protection point	13.3V	14.5V
+12VSB over voltage protection point	13.3V	14.5V

Note: +12VSB OVP test is under PSOFF or PSON state with Main output min load condition.

5.4 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically. The OTP circuit has built in a margin such that the power supply will not oscillate on and off due to temperature recovering condition.

Table 22 Over Temperature Protection Trip Levels

Over temperature warming, hot spot point (OTW)	105°C
Over temperature shut down, hot spot point (OTP)	115°C

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



6. Control Signals

The following sections define the input and output signals from the power supply.

Signals that can be defined as low active use the following convention: Signal# = low active.

6.1 PS_ON# Input Signal (Pin A21)

The PS_ON# signal is required to remotely turn on/off the power supply. PS_ON# is an active low signal that turns on Main output power rail. When this signal is not pulled low by the system, or left open, the outputs turn off.

This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Table 23 for the PS_ON# signal characteristics.

Table 23 PS_ON# Signal Characteristics

Signal Type (Active Low)	Pull-high to 3.3V with inner 3.48K ohm resistor	
PS_ON# = Low	ON	
PS_ON# = High or Open	OFF	
	Min.	Max.
Logic level low (power supply ON)	0V	1V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, PS_ON# = Low		4.0 mA
PS_ON# rise and fall time		100μsec

6.2 PWOK (Power OK, Pin A25)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit. Refer to Table 24 for the PWOK signal characteristics.

Table 24 PWOK Signal Characteristics

Signal Type	Pull-high to 3.3V with inner 0.02K ohm resistor	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	Min	Max.
Logic level low voltage	0V	0.4V
Logic level high voltage	2.4V	3.46V
Sink current, PWOK = low		4mA
Source current, PWOK = High		400μA
PWOK rise and fall time		100μsec

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



6.3 SMBAlert# (Pin A22)

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Amber or blink Amber. Refer to Table 25 for the SMBAlert# signal characteristics.

Table 25 SMBAlert# Signal Characteristics

Signal Type (Active Low)	Pull-high to 3.3V with inner 1K ohm resistor	
SMBAlert# = High	Power OK	
SMBAlert# = Low	Power Not OK	
	Min.	Max.
Logic level low voltage	0V	0.4V
Logic level high voltage	2.4V	3.46V
Sink current, SMBAlert# = Low		4mA
Source current, SMBAlert# = High		50μA

6.4 RS- (Return Remote Sense, Pin A23)

The power supply has return remote sense (RS-) to regulate out ground drops in the system for the main output voltage.

6.5 RS+ (Main Output Remote Sense, Pin A24)

The power supply uses the remote sense (RS+) to regulate out Main output drops in the system for the main output voltage.

6.6 Cold Redundancy Bus (Pin B22, enable by system)

This pin is used in the Cold Redundancy mode control which all of Cold Redundancy Bus signals should be tied together. When the pin is HIGH in the Cold Redundancy mode, the slave power supply will enter the Cold Standby mode (sleep mode, Main output no output); and when the pin is LOW, the Cold Standby mode power supplies will in normal redundancy mode.

Cold Redundancy feature supports 1+1, 2+1, 3+1 and 2+2 redundant configurations. It uses the PMBus manufacturer specific command area to define PMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

6.7 PRESENT_N# (Pin B24)

This pin will be tied to Standby return through a resistor. System side should have a pull-up resistor which limits the max current 4mA to go through from this signal pin to the power supply, the pull-down resistor shall be 100 ohm with 1206/0805 package or short PRESENT# to ground directly.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



6.8 SDA (Pin A19)

Inner Pulled up Resistor to internal 3.3V = 49.9k ohm.

Inner serial Resistor (Rs) = 21 ohm.

6.9 SCL (Pin A20)

Inner Pulled up Resistor to internal 3.3V = 49.9k ohm.

Inner serial Resistor (Rs) = 22 ohm.

6.10 A0 (Pin B19)

Address Bit 0: Pull-up to PSU internal +3.3Vstby via 4.99k-ohm resistor.

6.11 A1 (Pin B20)

Address Bit 1: Pull-up to PSU internal +3.3Vstby via 4.99k-ohm resistor.

6.12 +12VLS (Pin B23)

This pin supports an active current sharing function for Main output by connecting all the same signals together.

Refer to Sec. 5.13 Load Sharing.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



7. ENVIRONMENTAL REQUIREMENTS

7.1 Temperature

Operating Ambient: 0°C to +50°C
Non-operating Ambient: -40°C to +70°C.

7.2 Humidity

Operating: 5% to 85% relative humidity (non-condensing)
Non-Operating: 5% to 95% relative humidity (non-condensing)

7.3 Altitude

Operating: To 5000 m;
Non-operating: To 15200 m;

7.4 Mechanical shock

Non-operating: 50 G Trapezoidal Wave, Velocity change = 170 in. / sec.
Three drops in each of six directions are applied to each of the samples.

7.5 Random vibration

Non-operating
Sine sweep:
5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points.
Random profile:
5Hz @ 0.01g²/Hz to 20Hz @ 0.02g²/Hz (slope up); 20Hz to 500Hz @ 0.02g²/Hz (flat);
Input acceleration = 3.13gRMS; 10 min. per axis for 3 axes on all samples.

7.6 Thermal Shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. $\geq$ transition time $\geq$ 15°C/min.,
duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072



8. FIRMWARE REQUIREMENTS

8.1 General Description

8.1.1 Scope

The communication follows the Power System Management Protocol Specification (PMBus V1.2) for power support with regard to PSU to system communication, command and control. Not all PMBus functions are supported. The PEC byte must be included.

The PSU status registers must reflect the current working status of the PSU in real time. The registers should also be recovered after the PSU protection status is recovered.

8.1.2 Reference Documents

PMBus Application Profile for AC/DC Server Power Supplies, Revision 1.2; Oct 31, 2012.
(Intel Reference Number: 451620)

PMBus Power system management protocol Specification (V1.2) Part I and Part II.

System Management Bus (SMBus) Specification, Revision 2.0; Aug 3, 2000

8.1.3 Reference Information

8.1.3.1 Numerical Formats

Decimal numbers are indicated by either the suffix 'of' or the lack entirely (e.g. 1234d, 1234). Hex numbers are indicated by the prefix '0x' or the suffix 'h' (e.g. 0xAB, ABh).

Binary numbers are indicated by the suffix 'b' (e.g. 11010011b).

8.1.3.2 Signal Names

Signals that are active Low are indicated by either the '#' suffix (e.g. SMBALERT#).

8.1.3.3 Bit and Byte Order

When data is transmitted, the lowest order byte is sent first and the highest order byte is sent last.

Within any byte, the most significant bit (MSB) is sent first and the least significant bit (LSB) is sent last.

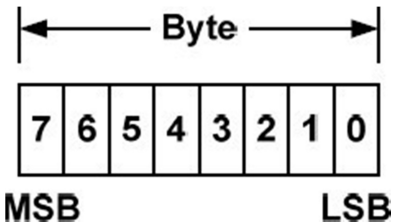


Figure 12 Bit Order within a Byte

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

8.1.4 Alert Response Address (ARA) Support

Alert Response Address feature (ARA) defined in the SMBus spec is not supported.

8.1.5 Abbreviations, Acronyms, and Definitions

Table 28 Abbreviations, Acronyms, and Definitions	
Term	Definition
PMBus	Power Management Bus Standard
SMBus	System Management Bus Standard
DSP	Digital Signal Processor
S	Start of I ² C Communication
P	Stop of I ² C Communication
ACK	Acknowledge. The response from a receiving unit indicating that it has received a byte.
NACK	Not acknowledge. The response from a receiving unit indicating that it has received invalid data.
ISP	In-System Programming
PEC	Packet Error Checking
RO	Read-Only capable
RW	Read/Write capable
PSU	Power Supply Unit
BMC	Baseboard Management Controller
ME	Management Engine
Assert, Asserted	A signal is asserted when the signal is true.
De-assert, De-asserted	A signal is de-asserted when the signal is false.
POR	Power on reset.

8.1.6 Data Formats

8.1.6.1 Linear Data Format

Real Data Relation to Linear format is: $X = Y \cdot 2^N$

X = the “real world” value in volts, amps, watts, degrees C, RPM or time durations

Y = two’s complement integer mantissa

The mantissa is the variable components that changes as the sensor value changes.

N = two’s complement integer exponent

8.1.6.1.1 Current, input voltage, power, temperature, fan speed, percentage and time duration

PMBUS V1.2 commands related to current, input voltage, power, temperature and fan speed shall use the PMBUS V1.2 Linear-11 data format.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072

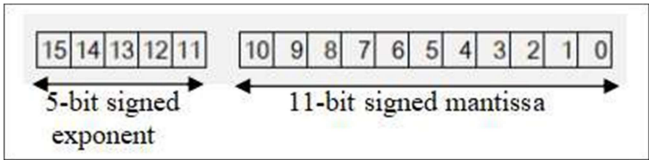


Figure 13 Linear-11 Format

8.1.6.1.2 Output voltage related commands

PMBUS V1.2 commands related to output voltage shall use the Linear-16 mode format (The exponent for all output voltage-related commands (e.g. READ_VOUT) is fixed at “-9”. The real value (X) = $Y \times 2^{-9}$ where Y = mantissa

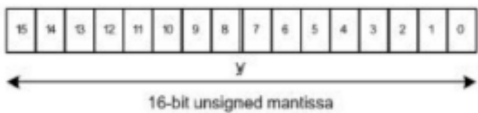


Figure 14 Linear-16 Format

8.1.7 Bus Speed

The PSU works in standard mode (max bus speed is 100 kHz). Electrical characteristics and SCL / SDA timing specification please refer “System Management Bus (SMBus) Specification, Revision 2.0; Aug 3, 2000”.

8.1.8 Device Base Addressing

The PSU PMBus device address locations are shown below. For redundant systems there are two signals to set the address location of the PSU once it is installed in the system; Address1, Address0.

Table 29

Address1/Address0	0/0	0/1	1/0	1/1
PMBus Address W/R	B0h/B1h	B2h/B3h	B4h/B5h	B6h/B7h
EEPROM Address W/R	A0h/A1h	A2h/A3h	A4h/A5h	A6h/A7h

8.2 Application Layer Requirements

The application layer is based upon PMBus specification rev 1.2. The PSU should conform to these specifications. Additional requirements, exceptions to, and clarifications of the PMBus specification are detailed in this section.

8.2.1 PSU Parameter Measurement and Reporting Accuracy

The sensor commands shall meet the following accuracy requirements. 100% load is based on high line max load.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 30 Power Supply Measurement Accuracy Requirements

Command	Pout<5%	5%≤ Pout <10%	10%≤Pout<20%	20%≤Pout≤100%
READ_VIN	±5%	±5%	±5%	±2%
READ_IIN	±0.2A or ±10% whichever is greater when Iin < 0.2A, report 0.2A	±0.2A or ±10% whichever is greater	±5%	±2%
READ_PIN	±10W or ±10% whichever is greater when Pin≤10W, report 10W	±5W or ±5% whichever is greater for models over 2000W; ±10W or ±5% whichever is greater	±5%	±2%
READ_VOUT	±5%	±5%	±5%	±2%
READ_IOUT	±1A or ±10% whichever is greater when Iout<1A, report 1A	±1A or ±10% whichever	±5%	2%
READ_POUT	±10W or ±10% whichever is greater when Pout≤7W, report 7W	±5W or ±5% whichever is greater for models over 2000W; ±10W or ±5% whichever is greater	±5%	2%

Note:

1. READ_IIN will be reset to 0.1A, and READ_PIN reset to 4W when PSU in cold redundant slave mode or DC-OFF line Standby mode; READ_IOUT and READ_POUT will be reset to 0 when PSU in cold redundant slave mode or DC-OFF line Standby mode.

Table 31 Other measurement accuracy

Command	Accuracy
TEMPERATURE	±3 (°C)
FAN SPEED	±500 (rpm)

Accuracy (%) = [|PMBus reading – Meter measurement| / Meter measurement]*100% Temperature accuracy:

| PMBus reading – Meter Measurement | ≤3°C

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.2.2 PMBus Command List

Table 32

Code	Range Value	Command	SMBus Transaction Type
03h	NA	CLEAR_FAULTS	Send Byte w/PEC
79h	NA	STATUS_WORD	Read Word w/PEC
7Ah	NA	STATUS_VOUT	Read Byte w/PEC
7Bh	NA	STATUS_IOUT	Read Byte w/PEC
7Ch	NA	STATUS_INPUT	Read Byte w/PEC
7Dh	NA	STATUS_TEMPERATURE	Read Byte w/PEC
81h	NA	STATUS_FANS_1_2	Read Byte w/PEC
86h	NA	READ_EIN	Block Read w/ PEC
87h	NA	READ_EOUT	Block Read w/ PEC
88h	NA	READ_VIN	Read word w/PEC
89h	NA	READ_IIN	Read word w/PEC
8Bh	NA	READ_VOUT	Read word w/PEC
8Ch	NA	READ_IOUT	Read word w/PEC
8Dh	NA	READ_TEMPERATURE_1 (Ambient)	Read word w/PEC
8Eh	NA	READ_TEMPERATURE_2 (Hot Spot)	Read word w/PEC
90h	NA	READ_FAN_SPEED_1	Read word w/PEC
96h	NA	READ_POUT	Read word w/PEC
97h	NA	READ_PIN	Read word w/PEC
98h	NA	PMBUS_REVISION	Read Byte w/PEC
99h	NA	MFR_ID	Block read w/PEC
9Ah	NA	MFR_MODEL	Block Read w/PEC
9Bh	NA	MFR_REVISION	Block Read w/PEC
9Ch	NA	MFR_LOCATION	Block Read w/PEC
9Dh	NA	MFR_DATE	Block Read w/PEC
9Eh	NA	MFR_SERIAL	Block Read w/PEC
A0h	NA	MFR_VIN_MIN	Read word w/PEC
A1h	NA	MFR_VIN_MAX	Read word w/PEC
A2h	NA	MFR_IIN_MAX	Read word w/PEC
A3h	NA	MFR_PIN_MAX	Read word w/PEC
A4h	NA	MFR_VOUT_MIN	Read word w/PEC
A5h	NA	MFR_VOUT_MAX	Read word w/PEC
A6h	NA	MFR_IOUT_MAX	Read Word w/PEC
A7h	NA	MFR_POUT_MAX	Read Word w/PEC
A8h	NA	MFR_TAMBIENT_MAX	Read Word w/PEC
A9h	NA	MFR_TAMBIENT_MIN	Read Word w/PEC

8.2.3 Bits Filed Define

Vin_UV_Warning, Vin_UV_Fault, Vin_OV_Fault, Pout_OP_Warning, Iout_OC_Warning, OT_Warning, OT_FAULT, Fan_Warning can be auto-recovered.

*Auto-recovered means the PSU, LED status and bit state can be reset while the abnormal condition return to normal condition.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 33 02h Command Table

02h	Bit Value	Meaning	Default
[7:6]	11	Reserved	10
	10	If bit 7 set, bit 6 clear, PSU ON/OFF controlled by the PSON# pin and OPERATION command bit [7].	
	01	If bit 7 clear, bit 6 set, PSU ON/OFF controlled by OPERATION command bit[6:5] only.	
	00	Reserved	
[5:4]	00	Reserved	00
3	0	Reserved	1
	1	PSU Turn off the output and stop transferring energy to the output as fast as possible response to the action control PSU off.	
[2:0]	000	Reserved	000

AUTO TURN ON (ON_OFF config and OPERATION)

The ON_OFF config command are used to turn the unit on and off in conjunction with PSON# and OPERATION command. The protection status and warning condition cannot be modified by the ON_OFF config.

- (1) When ON_OFF config command default status, PSU turn on/off by the control of PSON# and OPERATION command bit 7;
- (2) When ON_OFF config command set to disable PSON# function, PSU turn on/off by the control of OPERATION command bit[6:5].

- (3) PSU auto turn on function realized by 01h operation command and 02h ON_OFF config command.

For 01h operation command, valid data include 0x00h, 0x80h, 0x40h, 0x20h, any value not shown in the table is an invalid data, when write any invalid data, register will be reset to default value and declare a communications fault and respond as described in PMBus Specification.

For 02h ON_OFF config command, valid data include 0x88h, 0x48h, any value not shown in the table is an invalid data, when write any invalid data, register will be reset to default value and declare a communications fault and respond as described in PMBus Specification.

- (4) Each condition shown in the following 01h & 02h function table, assume PSU before status is ON status, 01h and 02h are default condition.
- (5) When PSU turn off by writing 0x48 to 02h, 0x40 to 01h, PSU will be auto turn on after the setting delay time, and register 01h command will be reset to default status, and 02h keep before status.
- (6) Auto turn on delay time default setting is 10s, and this time can be modified through PMBus command 60h, please refer 60h for detail.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 34 01h & 02h Function Table

02h (ON_OFF Config)					01h (ORERATION)				PS_ON#	Unit ON or OFF
Bits 7	Bits 6	Bits[5:4] (reserved)	Bits [3]	Bits [2:0]	Bits 7	Bits 6	Bits 5	Bits[4:0] (reserved)		
1 (default)	0 (default)	0 (default)	1 (default)	0 (default)	0 (default)	0 (default)	0 (default)	0 (default)	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU OFF
					1	0	0	0	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU ON
					0	1	0	0	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU OFF
					0	0	1	0	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU OFF
0	1	0	1	0	0 (default)	0 (default)	0 (default)	0 (default)	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU ON
					1	0	0	0	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU ON
					0	1	0	0	PS_ON# LOW	PSU turn off and then turn on auto after10s (10s is default)
									PS_ON# HIGH	
					0	0	1	0	PS_ON# LOW	PSU ON
									PS_ON# HIGH	PSU ON

Table 35 19h Command Table

19h	CAPABILITY			
Bits	Name	Value	Description	Default
7	Packet Error Checking	0	Packet Error Checking is not supported.	1
		1	Packet Error Checking is supported (default).	
6:5	Maximum Bus Speed	00	Maximum bus speed is 100 kHz (default).	00
		01	Maximum bus speed is 400 kHz (default).	
		10	Reserved	
		11	Reserved.	
4	SMBALERT#	0	There's no SMBALERT# pin and the SMBus Alert Response protocol is not supported.	1
		1	There's a SMBALERT# pin and the SMBus Alert Response protocol is supported (default).	
3:0	Reserved	0000	Reserved.	0000

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 36 1Ah command Table

1Ah	QUERY		
Bits	Value	Description	Default
7	1	Command is supported.	
	0	Command is not supported.	
6	1	Command is supported for write.	
	0	Command is not supported for write.	
5	1	Command is supported for read.	
	0	Command is not supported for read.	
4:2	000	Linear Data Format used	
	001	16 bit signed number	
	010	Reserved	
	011	Direct Mode Format used	
	100	8 bit unsigned number	
	101	VID Mode Format used	
	110	Manufacturer specific format used	
	111	Command does not return numeric data. This is also used for commands that return blocks of data.	
1:0	XX	Reserved for future use	00

Note: Only Read_Ein & Read_Eout support direct mode Format.

Table 37 3Ah command Table

3Ah	FAN_CONFIG_1_2		
Bits	Value	Description	Default
7	1	A Fan Is Installed In Position 1 (default)	1
	0	No Fan Is Installed In Position 1	
6	1	Fan 1 Is Commanded In RPM	0
	0	Fan 1 Is Commanded In Duty Cycle (default)	
5:4	00-11	Fan 1 Tachometer Pulses Per Revolution	01*
3	1	A Fan Is Installed In Position 2	0
	0	No Fan Is Installed In Position 2 (default)	
2	0	Not used	0
1:0	00	Not used	0

*It depends on revolution of fan selection.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 38 78h command STATUS_BYTE

78h	STATUS_BYTE			
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery
7	BUSY	"Not Implemented"	N/A	N/A
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	OFF	Yes, Reflects real time state of PSU
5	VOUT_OV_FAULT	An output over voltage fault has occurred.	Refer to STATUS_VOUT	No
4	IOUT_OC_FAULT	An output over current fault has occurred.	Refer to STATUS_IOUT	No
3	VIN_UV_FAULT	An input under voltage fault has occurred	Refer to STATUS_INPUT	Yes
2	TEMPERATURE	A temperature fault or warning has occurred.	Refer to STATUS_TEMPERATURE	Yes
1	CML	"Not Implemented"	N/A	N/A
0	NONE OF THE ABOVE		N/A	N/A

Note: bit 7 is NA, the PSU cannot be allowed to response busy state while the host is attempting to read/write from PMBus devices, The receiving device have to accept and process a communication over the bus.

Table 39 79h command STATUS_WORD

79h	STATUS_WORD (high byte)					
Bits	Name	Description	PSU state when bit is asserted ('1')	STATUS bit Auto Recovery	PAGE 00h(BMC) Default SMBAlert Mask value	PAGE 01h(ME) Default SMBAlert Mask value
7	VOUT	An output voltage fault or warning has occurred.	Refer to STATUS_VOUT	No	N/A	N/A
6	IOUT/P OUT	An output current or output power fault or warning has occurred	Refer to STATUS_IOUT	Refer to STATUS_IOUT	N/A	N/A
5	INPUT	An input voltage, input current, or input power fault or warning has occurred	Refer to STATUS_INPUT	Yes	N/A	N/A
4	MFR_SPECIFIC	A manufacture specific fault or warning has occurred.	Refer to STATUS_MFR_Spec	No	N/A	N/A
3	POWER_GOOD#	The POWER_GOOD signal, if present, is negated	Reflects real time state of PSU	Yes, reflects real time state of Power_Good#	N/A	N/A
2	FANS	A fan or airflow fault or warning has occurred	Refer to STATUS_FANS	Refer to STATUS_FANS	N/A	N/A
1	OTHER	"Not Implemented"	N/A	N/A	N/A	N/A

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

0	UNKN OW	"Not Implemented"	N/A	N/A	N/A	N/A
79h	STATUS_WORD (low byte)					
Bits	Name	Description	PSU state when bit is asserted ('1')	STATUS bit Auto Recovery	PAGE 00h(BMC) Default SMBAlert Mask value	PAGE 01h(ME) Default SMBAlert Mask value
7	BUSY	"Not Implemented"	N/A	N/A	N/A	N/A
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	OFF	Yes, reflects real time state of PSU	N/A	N/A
5	VOUT_O V_FAULT	An output over voltage fault has occurred	Refer to STATUS_VOUT	NO	N/A	N/A
4	IOUT_OC _FAULT	An output over current fault has occurred.	Refer to STATUS_IOUT	NO	N/A	N/A
3	VIN_UV_ FAULT	An input under voltage fault has occurred.	Refer to STATUS_INPUT	Yes	N/A	N/A
2	TEMPER ATURE	A temperature fault or warning has occurred.	Refer to STATUS_TEMPERATURE	Yes	N/A	N/A
1	CML	"Not Implemented"	N/A	N/A	N/A	N/A
0	NOTE OF THE ABOVE	"Not Implemented"	N/A	N/A	N/A	N/A

Note: bit 7 is NA, the PSU cannot be allowed to response busy state while the host is attempting to read/write from PMBus devices, The receiving device have to accept and process a communication over the bus.

Table 40 7Ah command STATUS_VOUT

7Ah	STATUS_VOUT				
Bits	Name	Description	PSU state when bit is asserted('1')	STATUS bit Auto Recovery	Default SMBAlert Mask value 1 = not cause assertion of SMBAlert#
					No Page
7	VOUT_OV_FAULT	Output Over voltage Fault	OFF	No	1
6	VOUT_OV_WARNING	"Not Implemented"	N/A	N/A	1
5	VOUT_UV_WARNING	"Not Implemented"	N/A	N/A	1
4	VOUT_UV_FAULT	Output Under voltage Fault	OFF	No	1
3	VOUT_MAX_WARNING	"Not Implemented"	N/A	N/A	1
2	TON				
1	TOF				
0	VOU				

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 41 7Bh command STATUS_IOUT

7Bh	STATUS_IOUT					
Bits	Name	Description	PSU state when bit is asserted '1'	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = not cause assertion of SMBAlert#	
					PAGE 00h (BMC)	PAGE 01h (ME)
7	IOUT_OC_FAULT	Output over current fault	OFF	No	0	0
6	Not implemented	"Not Implemented"	N/A	N/A	1	1
5	IOUT_OC_WARNING	Output over current warning	ON	Yes	0	0
4	Not implemented	"Not Implemented"	N/A	N/A	1	1
3	Not implemented	"Not Implemented"	N/A	N/A	1	1
2	Not implemented	"Not Implemented"	N/A	N/A	1	1
1	POUT_OP_FAULT	Output over power fault	OFF	No	1	1
0	POUT_OP_WARNING	Output overpower warning	ON	Yes	1	1

Note1: Yes means bit is de-asserted when the situation comes back to normal state. No means the bit keeps asserted when the PSU shutdown.

Table 42 7Ch command STATUS_INPUT

7Ch	STATUS_INPUT					
Bits	Name	Description	PSU state when bit is asserted '1'	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = not cause assertion of SMBAlert#	
					PAGE 00h (BMC)	PAGE 01h (ME)
7	VIN_OV_FAULT	Input over voltage Fault	OFF (Auto recovery)	Yes	1	1
6	VIN_OV_WARNING	*** Not implemented ***	N/A	N/A	1	1
5	VIN_UV_WARNING	Power Supply input out-of-range	ON	Yes	1	1
4	VIN_UV_FAULT	An input under voltage fault has occurred.	OFF (Auto recovery)	Yes	1	1
3	Unit Off for Low Input Voltage	Either the input voltage has never exceeded the input turn-on threshold or if the unit did start, the input voltage decreased below the turn-off threshold.	N/A	N/A	1	1
2	IIN_OC_FAULT	*** Not implemented ***	N/A	N/A	1	1
1	IIN_OC_WARNING	Input over current warning	ON	Yes	1	1
0	PIN_OP_WARNING	Input overpower warning	ON	Yes	1	1

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 43 7Dh command STATUS_TEMPERATURE

7Dh	STATUS_TEMPERATURE					
	Bits	Name	Description	PSU state when bit is asserted '1'	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = not cause assertion of SMBAlert#
						PAGE 00h (BMC) GE 01h(ME)
	7	OT_FAULTO	Over temperature fault	OFF(Auto _recovery)	Yes	0 0
	6	OT_WARNING	Over temperature warning	ON	Yes	0 0
	5	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	4	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	3	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	2	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	1	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	0	Not implemented	*** Not implemented ***	N/A	N/A	1 1

Table 44 7Eh command STATUS_CML

7Eh	STATUS_CML					
	Bits	Name	Description	PSU state when bit is asserted '1'	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = not cause assertion of SMBAlert#
						PAGE 00h(BMC) PAGE 01h (ME)
	7	Invalid/Unsupported Command	Slave received a invalid or unsupported command	ON	NO	1 1
	6	Invalid/Unsupported Data	Slave received a invalid or unsupported data	ON	NO	1 1
	5	Packet Error Check Failed	Slave received a error PEC code	ON	NO	1 1
	4	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	3	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	2	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	1	Not implemented	*** Not implemented ***	N/A	N/A	1 1
	0	Not implemented	*** Not implemented ***	N/A	N/A	1 1

Table 45 81h command STATUS_STATUS_FANS_1_2

81h	STATUS_FANS_1_2				
Bits	Name	Description	PSU state when bit is asserted‘1’	STATUS bit Auto Recovery	SMBALERT_MASK Default 0 = causes assertion of SMBAlert# 1 = not cause assertion of SMBAlert#
					PAGE 00h(BMC)
7	Fan 1 Fault	Fan 1 fault occurred.	OFF	No	1
6	Fan 2 Fault	*** Not implemented ***	N/A	N/A	1
5	Fan 1 Warning	Fan 1 warning occurred	ON	Yes	1
4	Fan 2 Warning	*** Not implemented ***	N/A	N/A	1
3	Fan 1 Speed Overridden	Fan 1 overridden occurred	ON	Yes	1

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



2	Fan 2 Speed Overridden	*** Not implemented ***	N/A	N/A	1
1	Not implemented	*** Not implemented ***	N/A	N/A	1
0	Not implemented	*** Not implemented ***	N/A	N/A	1

Note: The fan override bit can be set by command. The command has to be higher than the PSU itself. When the fan speed control is returned to PSU itself, the bit3 should be auto-recovery.

Table 46 80h command STATUS_MFR_Spec

80h	STATUS_MFR_Spec	
Bits	Name	Description PSU state when bit is asserted '1'
7	PFC OVP Fault	PFC OV fault occurred.
6	NA	*** Not implemented ***
5	NA	*** Not implemented ***
4	NA	*** Not implemented ***
3	NA	*** Not implemented ***
2	NA	*** Not implemented ***
1	DC input	Input Voltage is DC
0	AC input	Input Voltage is AC

Table 47 98h command PMBUS_REVISION

98h	PMBUS_REVISION		
Bits [7:5]	Part I Revision	Bits [3:0]	Part II Revision
000	1.0	000	1.0
001	1.1	001	1.1
010	1.2	010	1.2

Table 48 D2h Command Table

D2h	MFR_PSU_Defined		
Bits [7:5]	Input TYPE	111	AC+HVDC240V
		110	AC ONLY
		101	HVDC336V ONLY
		100	-48VDC
		011	AC+HVDC336V
		010	AC277V+HVDC336V
		001	HVDC240V
		000	Reserved
Bits [4:3]	FAN	11	XX
		10	FAN (air from AC connector to output connector)
		01	FAN (air from output connector to AC connector)
		00	FAN less
Bits [2:0]	Switch version		V1,V2 ~V7

Note: set to "000" if bits[2:0] is not applied.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 49 D9h Command Table

Byte	Value	Description
0	0-255	Minor revision; secondary
1	0-255	Minor revision; primary
2	0-255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0-> No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bite 0-6: Major revision (Major revision uses 0 during the development phase and starts with 1 after MP. Major version is carried when significant software change occurs.) The FW version on the PSU label is displayed in "major.primary.secondary" format. For example, major version is 01, primary version is 02, secondary version is 03. The FW version on the PSU label should be displayed as "01.02.03". The FW version on the PSU label is displayed in three segments. Each segment is a hexadecimal number, and the letters should be capitalized. Each segment must have two digits. If the number of digits is insufficient, use leading zeros to fill. For example, 11.0A.21, 0B.00.00, 00.22.EE.

Table 50 EAh Command FW SPEC

EAh	FW SPEC
Tencent V1	PSU conforms to Tencent V1 SPEC
Others	Reserved

9.2.4 Reset of Status Bits

The STATUS_ commands shall be reset only by the below methods. If the event is still present that caused the assertion of the status bit, the bit shall stay assert after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.
- Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'. CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
- Cycling input power OFF for 1 second or more then ON shall reset all STATUS_ bits to '0'.
- Systems with redundant power supplies where only one of the supplies cycle input power OFF/ON; the power cycled PSU shall reset the STATUS_ bits to '0' only when powered back ON. If the PSU is kept OFF, the STATUS_ bits shall not be reset.
- Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall be reset only on the assertion of PSON#; not the de-assertion.
- While the communication failure occur, the PSU should have the ability to reset its own I²C module. PSU should not reset I²C bus at any time.

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

8.2.5 SMBALERT#

SMBALERT# is a signal (active low) sourced by the PSU to indicate when a STATUS register bit assertion has taken place. If one STATUS bit asserts (sets to '1') while its corresponding SMBALERT_MASK bit is cleared to '0', then an SMBALERT# signal must be driven and remain asserted as long as the underlying condition exists. The SMBALERT_MASK default values are such that only STATUS_ bits asserted within PAGE 01h (ME) instance will generate SMBALERT#. And by default the SMBALERT# signal is asserted for the following cases in FW default design.

[1] STATUS_IOUT (Iout OC Warning / Iout OC fault)

[2] STATUS_TEMPERATURE (OT Warning / OT fault)

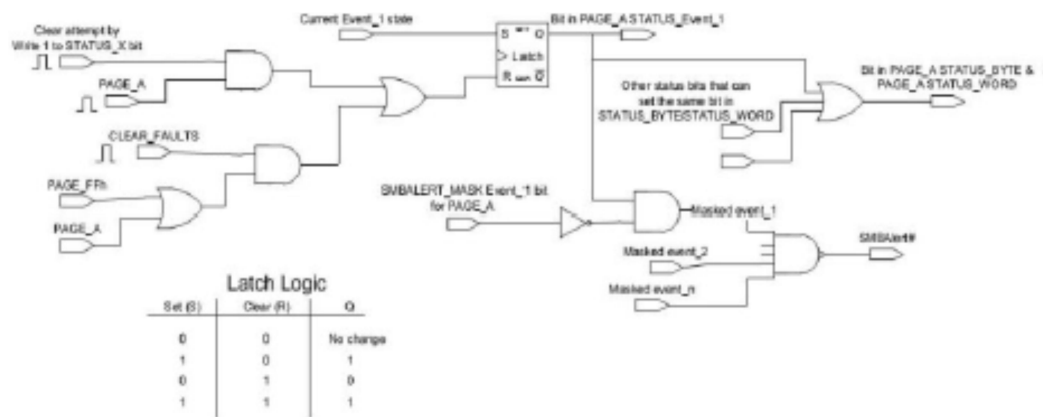


Figure 15 Conceptual Schematic of STATUS Bits and SMBALERT# for commands that support PAGE_PLUS_

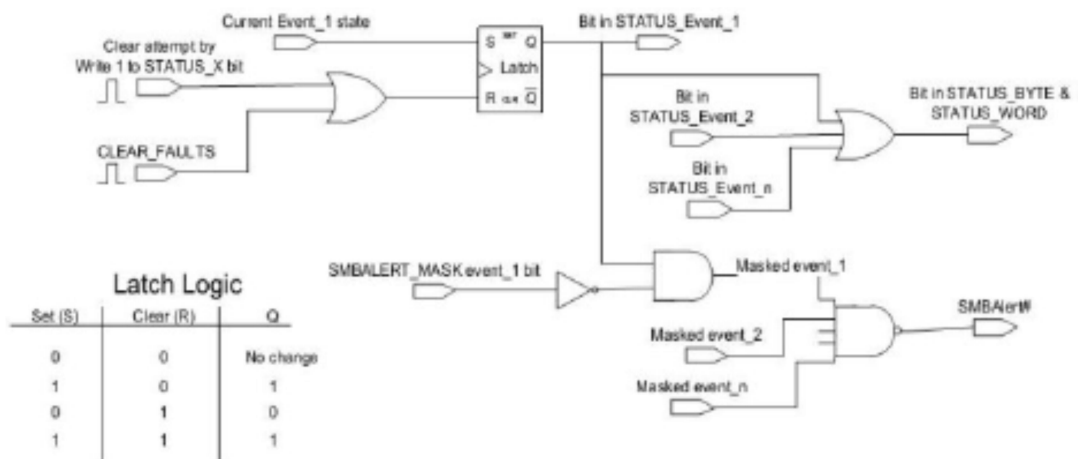


Figure 16 Conceptual Schematic of STATUS Bits and SMBALERT# without PAGE_PLUS_

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.2.6 FRU Requirements

8.2.6.1 FRU Data

The FRU data format shall be compliant with the IPMI ver.1.2 specification. The current version of these specifications is available at <http://developer.intel.com/design/servers/ipmi/spec.htm>. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

8.2.6.2 FRU Device Protocol

The FRU device will implement the same protocols as the commonly used AT24C02 device, including the byte read, sequential read, byte write, and page read protocols.

8.2.6.3 FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 51

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document.
Product information shall be defined as follows:	
Manufacturer Name	{Formal name of manufacturer}
Product Name	{Manufacturer's model number}
Product part/model number	Customer part number
Product Version	Customer current revision (HW version)
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	{Not required}
PAD Bytes	reserve
Multi-Record Area	reserve
Multi-Record information shall be defined as follows:	
Field Name (PS Info)	Field Information Definition
Overall Capacity (watts)	reserve
Peak VA	reserve
Inrush current (A)	reserve
Inrush interval (ms)	reserve
Low end input voltage range 1	reserve
High end input voltage range 1	reserve
Low end input voltage range 2	reserve
High end input voltage range 2	reserve
A/C dropout total. (ms)	reserve
Binary flags	reserve
Peak Wattage	reserve
Combined wattage	reserve
Predictive fail tach support	reserve

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W Manufacturer Part No.: KS260072

Field Name (Output)	reserve
Output Information	reserve
All other output fields	reserve

8.2.6.4 FRU Write Protection

The contents of the FRU shall have write protection using the PMBus command MFR_FRU_PROTECTION with the hexadecimal number DBh using Write Byte and Read Byte types of commands with PEC. A read value of 00h means the FRU can be written and a value of 01h means the device can’t be written (write protection activated), same values apply for Write operation

8.3 CR & OFF Line Mode

This is a common specification defining Cold Redundancy 2 requirements uses in redundant power supplies. It covers both power supply and system requirements supporting redundant configurations. Cold Redundancy uses the PMBus manufacturer specific command area to define SMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring. PSU in standby mode should not turn off Main output.

8.3.1 Cold Redundancy Configuration

Table 52

Cold_Redundancy_Config (D0h)		
Value	State	Description
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply’s CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
06h - FFh	reserved	

[1] Redundancy mode

D0h is 0x00 (Default)

[2] Active – Always Standby mode

Example: System commands D0h is 0x01 (Active PSU) or 0x05 (Always Standby PSU)

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



1. To set one PSU is Active, CR-pin out would be turned to high from low level immediately.
2. The other PSU is set to standby mode and enter to Sleep quickly.
3. Standby PSU should take over immediately within 100us while the Active PSU is AC lost or failure, to maintain the system loading. The output voltage on the bus cannot be out of regulation in this case.

[3] Cold Redundant mode

Example: System command one is Active (0x01), the others are Cold Standby (0x02, 0x03, 0x04)

1. To set one PSU is Active, CR-pin out would be turned to high from low level immediately.
2. All PSU would depend on the system load, to turn on or turn off the other slave PSUs. System Load < (TBD), CR pin is still high, PSU2 sleep.
System Load > (TBD), CR pin is still high, PSU2 wake up.
3. While the master PSU is AC lost or failure, CR pin have to be turned to low quickly, to wake up the other slave PSUs within 100us. To maintain the system loading is working continuously. Also, the output voltage on the bus cannot be out of regulation in this case.

[4] When system command CR or active – always Standby mode condition, the PSU in sleep mode have the following feature:

1. LED status is changed to Flashing green (0.5sec on/0.5sec off, 1Hz blinking green)
2. PMBus Iout & Pout report 0.
3. When AC off or Input_UV, the LED should be amber.
4. E1h value, total 7 bytes (optional).
5. According to the total quantity at cold redundant (such as D0h is 2, 3 or 4), PSU have to define the different optimized Von /Voff point. The purpose is target the best efficiency performance for total power consumption at each CR mode.
6. During system command period for CR or active – always Standby mode, cannot cause system shutdown or damage.
7. While any PSU in Cold Redundant mode is AC lost or failure, CR pin should be turned to low quickly, to wake up the other PSUs to normal mode.
8. The output voltage on the bus cannot be out of regulation.

8.3.2 Power On/Off of Power Supplies in Cold Redundant Mode

Table 53 Protocol of Von/Voff Configure command

Command Code	Command Name	Read/Write	Number of Data Bytes
E1h	Von/Voff Configure	Block R/W	6

- Write command:

S Address/W E1 06 Von2 Voff2 Von3 Voff3 Von4 Voff4 PEC

- Read command:

S Address/W E1 Address/R 06 Von2 Voff2 Von3 Voff3 Von4 Voff4 PEC

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

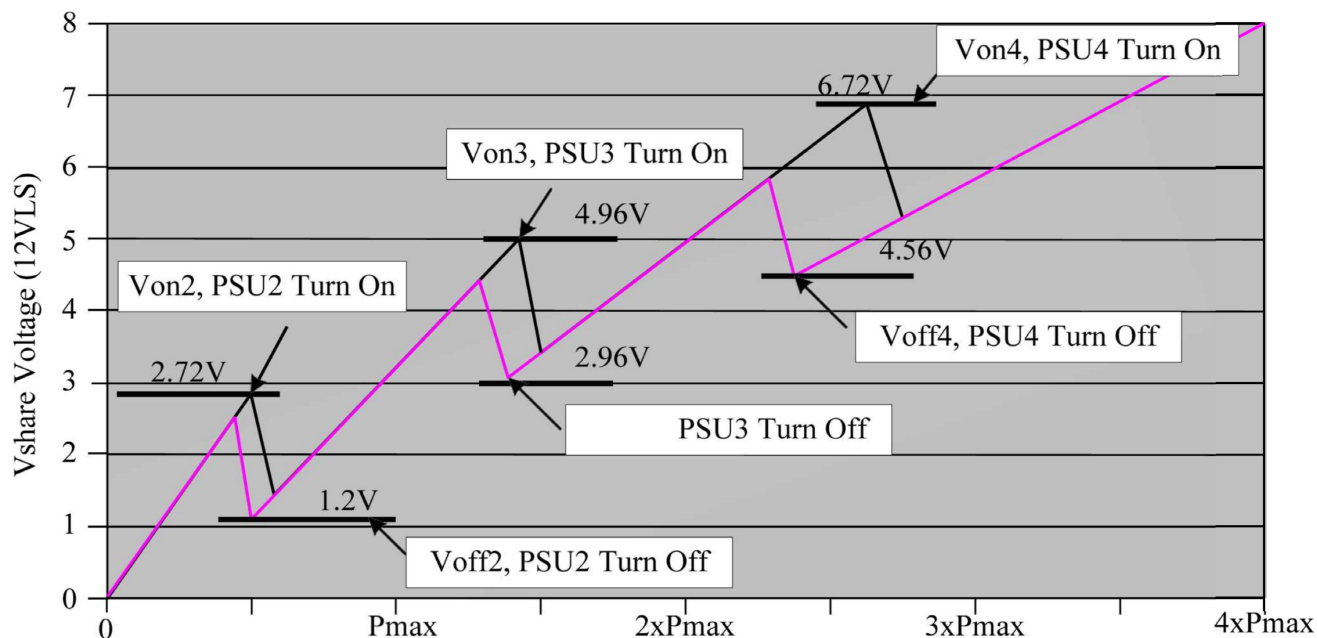


Figure 17 Example Power On/Off of Power Supplies in Cold Redundant Mode

Von2: more than this load the cold standby PSU2 will be wake up.

Voff2: less than this load the cold standby PSU2 will sleep.

Von3: more than this load the cold standby PSU3 will be wake up.

Voff3: less than this load the cold standby PSU3 will sleep.

Von4: more than this load the cold standby PSU4 will be wake up.

Voff4: less than this load the cold standby PSU4 will be sleep.

8.4 Query(1Ah)

Table 54

CMD Code	Command Name	bit7 1: support 0: not support	bit6 1: support to write 0: not support to write	bit5 1: Support to read 0: not support to read	bit4-bit2 000: Linear 011: Direct	bit1-bit0
00h	PAGE	1	1	1	100	00
01h	OPERATION	1	1	1	111	00
02h	ON OFF Config	1	1	1	111	00
03h	CLEAR_FAULTS	1	1	0	111	00
05h	PAGE_PLUS_WRITE	1	1	0	111	00
06h	PAGE_PLUS_READ	1	0	1	111	00
19h	CAPABILITY	1	0	1	111	00
1Ah	QUERY	1	0	1	111	00
1Bh	SMBALERT_MASK	1	0	1	111	00
20h	VOUT_MODE	1	0	1	111	00
30h	COEFFICIENT	1	0	1	111	00

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

3Ah	FAN_CONFIG_1_2	1	0	1	111	00
3Bh	FAN_COMMAND_1	1	1	1	000	00
60h	AUTO_TURNON_DELAY	1	1	1	111	00
78h	STATUS_BYTE	1	0	1	111	00
79h	STATUS_WORD	1	0	1	111	00
7Ah	STATUS_VOUT	1	0	1	111	00
7Bh	STATUS_IOUT	1	0	1	111	00
7Ch	STATUS_INPUT	1	0	1	111	00
7Dh	STATUS_TEMPERATURE	1	0	1	111	00
7Eh	STATUS_CML	1	0	1	111	00
80h	Status_MFR_Spec	1	0	1	111	00
81h	STATUS_FANS_1_2	1	0	1	111	00
86h	READ_EIN	1	0	1	011	00
87h	READ_EOUT	1	0	1	011	00
88h	READ_VIN	1	0	1	000	00
89h	READ_IIN	1	0	1	000	00
8Ah	READ_VCAP	1	0	1	111	00
8Bh	READ_VOUT	1	0	1	000	00
8Ch	READ_IOUT	1	0	1	000	00
8Dh	READ_TEMPERATURE_1	1	0	1	000	00
8Eh	READ_TEMPERATURE_2	1	0	1	000	00
8Fh	READ_TEMPERATURE_3	1	0	1	000	00
90h	READ_FAN_SPEED_1	1	0	1	000	00
96h	READ_POUT	1	0	1	000	00
97h	READ_PIN	1	0	1	000	00
98h	PMBUS_REVISION	1	0	1	111	00
99h	MFR_ID	1	0	1	111	00
9Ah	MFR_MODEL	1	0	1	111	00
9Bh	MFR_REVISION	1	0	1	111	00
9Ch	MFR_LOCATION	1	0	1	111	00
9Dh	MFR_DATE	1	0	1	111	00
9Eh	MFR_SERIAL	1	0	1	111	00
9Fh	APP_PROFILE_SUPPORT	1	0	1	111	00
A0h	MFR_VIN_MIN	1	0	1	000	00
A1h	MFR_VIN_MAX	1	0	1	000	00
A2h	MFR_IIN_MAX	1	0	1	000	00
A3h	MFR_PIN_MAX	1	0	1	000	00
A4h	MFR_VOUT_MIN	1	0	1	000	00
A5h	MFR_VOUT_MAX	1	0	1	000	00
A6h	MFR_IOUT_MAX	1	0	1	000	00
A7h	MFR_POUT_MAX	1	0	1	000	00
A8h	MFR_TAMBIENT_MAX	1	0	1	000	00
A9h	MFR_TAMBIENT_MIN	1	0	1	000	00
AAh	MFR_EFFICIENCY_LL	1	0	1	000	00
ABh	MFR_EFFICIENCY_HL	1	0	1	000	00
C0h	MFR_MAX_TEMP_1	1	0	1	000	00
C1h	MFR_MAX_TEMP_2	1	0	1	000	00
C2h	MFR_MAX_TEMP_3	1	0	1	000	00
D0h	CR_Mode	1	1	1	111	00

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

D2h	MFR_PSU_Defined	1	0	1	111	00
D4h	MFR_HW_COMPATIBILITY	1	0	1	111	00
D5h	MFR_FWUPLOAD_CAPABILITY	1	0	1	111	00
D6h	MFRY_FWUPLOAD_MODE	1	1	1	111	00
D7h	MFR_FWUPLOAD	1	1	0	111	00
D8h	MFR_FWUPLOAD_STATUS	1	0	1	111	00
D9h	FW REVISION	1	0	1	111	00
DBh	FW write protection	1	1	1	111	00
DCh	MFR_BLACKBOX	1	0	1	111	00
DDh	MFR_REAL_TIME_BLACK_BOX	1	1	1	111	00
DEh	MFR_SYSTEM_BLACK_BOX	1	1	1	111	00
DFh	MFR_BLACKBOX_CONFIG	1	1	1	111	00
E0h	MFR_CLEAR_BLACKBOX	1	1	0	111	00
E1h	CR VonVoff	1	1	1	111	00
E2h	PSU units	1	1	1	111	00
E3h	OUTPUT COUNT	1	0	1	111	00
EAh	FW_SPEC	1	0	1	111	00

8.5 Black Box

This specification defines the requirements for power supplies with PMBus capability to store PMBus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shut-down. The data can be accessed via the PMBus interface by applying power to the 12VSB pins. No AC power need to be applied to the power supply.

8.5.1 When Data is saved to the Black Box

Data is saved to the Black Box for the following fault events:

- General fault (Other faults that lead to PSU shutdown)
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

Note: Data should be saved to the black box when the same type of fault occurs continuously.

8.5.2 Black Box Events

There are two types of data saved in the black box:

- 1) System Tracking Data
- 2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.5.3 Black Box Process

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks number of PSON and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM.
- Power supply loads warnin and fault event counter data from EEPROM into RAM.
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM.
- Upon a fault event that causes the PSU to shut-down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC and PSON power cycles, PSU ON time, warning event counters and fault event counters.

8.5.4 Commands

8.5.4.1 MFR_BLACKBOX(0xDC)

Format: Read Block with PEC (238 bytes)

Table 55

Type	Item	Bytes	Description
System Tracking Data 47	System top assembly number	10	ASCII
	System serial number	10	
	Motherboard assembly number	10	ASCII
	Motherboard serial number	10	
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute
	Present number of AC power cycles	2	
	Present number of PSON power cycles	2	
Power supply event data (N)		38	Most recent occurrence of saved black box data
Event Data Time Stamp 11	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute
	Real Time Clock Data from System	4	This time stamp does not need to generated by the power supply. The system rights a real time clock value eriodically to the power supply using the MFR_REAL_TIME command. LSB = 1 second
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



EventData PMBus 22	STATUS_WORD	2	The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Data Event	AC Loss	1	The power supply shall save a count of these critical events to non-volatile memory each
	OTP		
Counters 5	OCP/OPP	1	time they occur. The counters will increment each time the associated STATUS bit is asserted. (Once a value has reached 15, it shall stay at 15 and not reset.)
	General failure shutdown		
	Fan failure	1	
	OVP		
	Input voltage warning; no shutdown	1	
	Thermal warning; no shutdown		
	Output current power warning; no shutdown	1	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit, the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Fan slow warning;no shutdown		

8.5.4.2 MFR_REAL_TIME_BLACK_BOX (0xDD)

Format: Write/Read Block with PEC (4 bytes)

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1s resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C. For example, BMC sends "0x04 (length) 0x04 0x03 0x02 0x01", when the real-time is 0x01020304. When BMC reads data from PSU, PSU returns "0x04 (length) 0x04 0x03 0x02 0x01".

8.5.4.3 MFR_SYSTEM_BLACK_BOX (0xDE)

Format: Write/Read Block with PEC (40 bytes). Low byte first.

The system uses this command to write the following data to the PSU.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W Manufacturer Part No.: KS260072



Table 56

Item	Bytes	Description
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High Bytes

8.5.4.4 MFR_BLACKBOX_CONFIG (0xDF)

Format: Read/Write Byte with PEC

Table 57

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box funciton enabled; bit0 = 1
1-7		reserved

8.5.4.5 MFR_CLEAR_BLACKBOX (0xE0)

Format: Send Byte with PEC

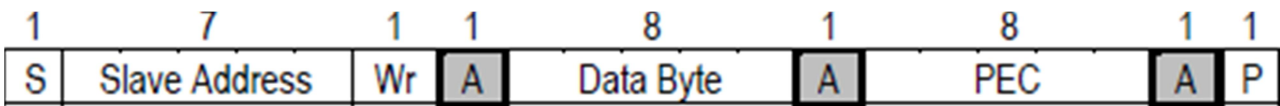


Figure 18 Send Byte Protocol with PEC

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously. This command is write only. There is no data byte for this command.

8.6 Firmware Update

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the primary and secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the OFF state. All firmware updates include primary side and secondary side. There is no firmware update including separate primary side or separate secondary side. PSU should run the last FW version or initial FW version while the bootloader fail since AC power is removed during FW update process and so on.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.6.1 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1. Boot Loader: This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling and PFC OVP.

2. Main Program: This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

8.6.2 Summary of Commands and Capabilities Supported in Boot Loader Mode

When the power supply is in FW Upload mode the following commands shall be supported.

Table 58

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte with PEC
1Ah	QUERY	Block Write Block Read Process Call with PEC
98h	PMBUS_REVISION	Read Byte with PEC
9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word with PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte with PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte with PEC
D7h	MFR_FWUPLOAD	Block Write with PEC(size = block size from image header)
D8h	MFR_FWUPLOAD_STATUS	Read Word with PEC
D9h	MFR_FW_REVISION	Block Read with PEC(3 bytes)

Basic Function	Operating Capability
Fan control	Fan can run to make sure power supply is cooled in the system for the duration to the FW update.
PWOK	The PWOK signal must still function properly during power on/off cycles to reset the system

8.6.3 Power Supply Operating Mode During and After Firmware Update Firmware update mode in OFF state with no power cycle needed:

Power supply may be able to support FW upload in the OFF state. The new FW will take effect once it is taken out of FW upload load.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Bad image after firm. The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode, the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

8.6.4 Firmware Image Header

Table 59

Image header			Comment
Byte0	[0:7]		CRC Low Byte
Byte1	[0:7]		CRC High Byte
Byte2~9		Image information	
Byte10~20		Product model name, reserved"00" for no use bytes, ASCII format. Fill MFR_MODEL from back to front into Byte10~20. E.g., the MFR_MODEL is "abcdefghijk-mn", byte10 is "d", byte11 is "e", ... , byte20 is "n".	
Byte21~22	[0:7]	For future use	
	[0:7]	For future use	
Byte23	[7]	down revision control bit	
	[0:6]	Major version	
Byte24	[0:7]	FW_MINOR_PRIMARY (not used by system)	
Byte25	[0:7]	FW_MINOR_SECONDARY	
Byte26	[0:7]	HW_COMPATIBILITY_FIRST	
Byte27	[0:7]	HW_COMPATIBILITY_SECOND	
Byte28	[0:7]	BLOCK SIZE Low Byte	
Byte29	[0:7]	BLOCK SIZE High Byte	
Byte30	[0:7]	Write Time Low Byte	Unit: ms
Byte31	[0:7]	Write Time High Byte	

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.6.5 PSU Upload Process

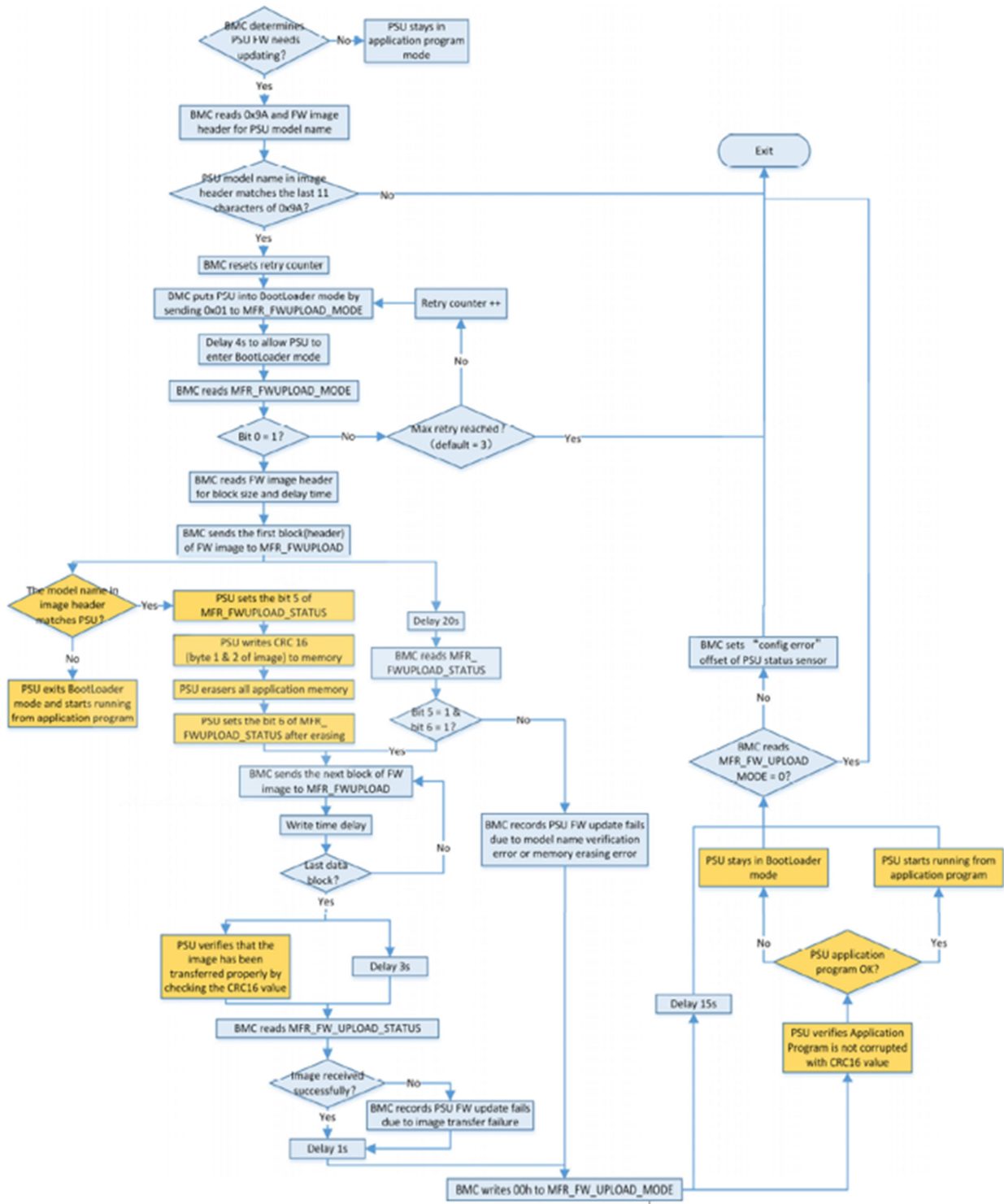


Figure 19 PSU Upload Process

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

8.6.6 PSU Flow During Powering ON

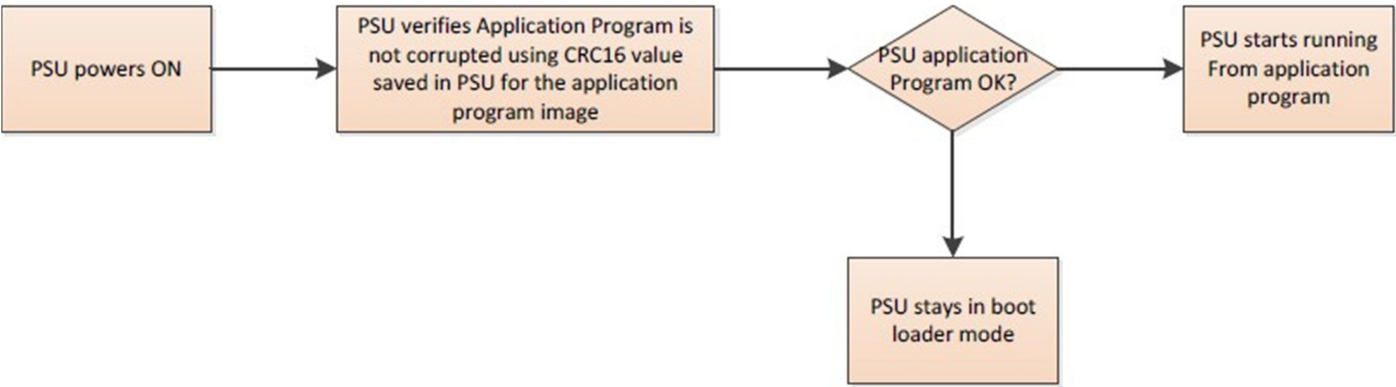


Figure 20

8.6.7 Power Supply Commands

Name: MFR_HW_COMPATIBILITY
 Format: Read Word

Table 60

Code: D4h Bytes	Value	Description
low	ASCII code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCII code for second letter/number of the PSU HW compatibility.	

Name: MFR_FWUPLOAD_CAPABILITY
 Format: Read Byte
 Code: D5h
 The system can read the power supply’s FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Table 61

Bit	Value	Description
0	1 = PSU support FW uploading in standby mode only	For future use
1	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

SWITCHING POWER SUPPLY



CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

Code: D6h

Table 62

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the first image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restart This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1	0 = the application memory has not been erased. 1 = the application memory has been erased.	PSU sets this bit after the application memory is cleared. PSU resets this bit after the FW update gets completed.
2-7		Reserved

Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

Table 63

Bytes	Value	Description
Block size defined in header	Image header and image data	Command used to send each block of the FW image. Header should follow the format described in Section 10.5.5. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.

Reset: All bits get reset to 0 when the power supply enters FW upload mode.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



Table 64

Bit	Description
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5	0 = The model name in image header does not match PSU. 1 = The model name in image header matches PSU.
6	0 = The application memory has not been erased. 1 = The application memory has been erased.
7-15	Reserved

Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: D9h

Table 65

Byte	Value	Description
0	0-255	Minor revision; secondary
1	0-255	Minor revision; primary
2	0-255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed but recommended to follow. 0 No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



8.7 Filtering and Delay

8.7.1 Filter processing

The firmware should take filtering as essential steps in the analog signal's sampling process, meanwhile with the delay for the judge process, in order to avoid corresponding signal's accidental assert and so on.

- The common filtering methods as follows:

1. Average Filter

$$Y_n = \sum_{i=1}^n X_i / N$$

①

Sampling multiple samples, then calculating the average to implement the filtering process

2. Limiting Filter

$$\Delta E = Y_n - Y_{n-1} \quad (* \Delta E \in (0, \Delta E_{\max})) \quad ②$$

First define a maximum error value, e.g. $\Delta E_{\max}$, and use this to limit the difference between the adjacent two sampling results (as formula ②).

3. Low Pass Filter

$$Y_n = a * X_n + (1 - a) * Y_{n-1} \quad (a \in (0, 1)) \quad ③$$

Filtering the original sampled data by adjusting the low-pass filter factor.

8.7.2 Delay Processing

In the judgment and similar process, it is necessary to make the hysteresis to ensure the consistency of timing in the corresponding logic, the sketch map as below.

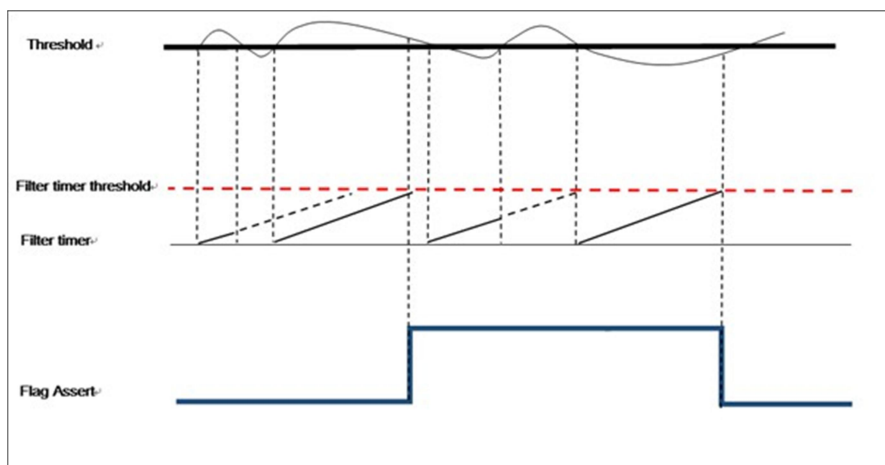


Figure 21

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



9. RELIABILITY

9.1 Component De-rating

Refer to latest version of component derating guide. Any exceptions are subject to final approval.

9.2 Electrolytic Capacitor Life Requirement

The E-CAP life shall be greater than 44,000 hours or 5 years under the following conditions: Input

Voltage: 230 VAC.

Output Load: 70% load. Ambient

Temperature: 50°C.

9.3 Fans

The used fan must have a L10 lifetime of 70,000h at 40°C ambient temperature of the power supply with 100% load at PSU.

9.4 Mean Time Between Failures (MTBF)

The power supply shall have a minimum CMTBF at continuous operation of 100,000 hours at 100% load and 25°C, as calculated by Telcordia SR-332 Issues 2.

10. PRODUCT SAFETY AND EMC COMPLIANCE

10.1 Product Safety Compliance

IEC60950-1 (International)

IEC62368-1 (International)

CE- Low Voltage Directive 2014/35/EU

GB4943.1-2022

10.2 Product EMC Compliance

EN55032

EN55035

- ☐ EN61000-4-2 Electrostatic Discharge
- ☐ EN61000-4-3 Radiated RFI Immunity
- ☐ EN61000-4-4 Electrical Fast Transients
- ☐ EN61000-4-5 Electrical Surge
- ☐ EN61000-4-6 RF Conducted Immunity
- ☐ EN61000-4-8 Power Frequency Magnetic Fields

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



☐ EN61000-4-11 Voltage Dips and Interruptions

☐ EN61000-3-2 - Harmonics (Europe)

EMC Directive 2014/30/EU

GB/T9254.1-2021 (EMC)

GB 17625.1-2022 (Harmonics)

10.3 Dielectric Withstand (Hi-pot)

Input to earth ground 1500Vac or 21500Vdc for 1 minute, less than 10mA leakage.

Primary to secondary 3000Vac or 4242Vdc for 1 minute, less than 30mA leakage.

Primary to secondary 500Vdc for 1 minute, isolation resistance shall not be less than 2Mohm.

10.4 Leakage (Touch) Current

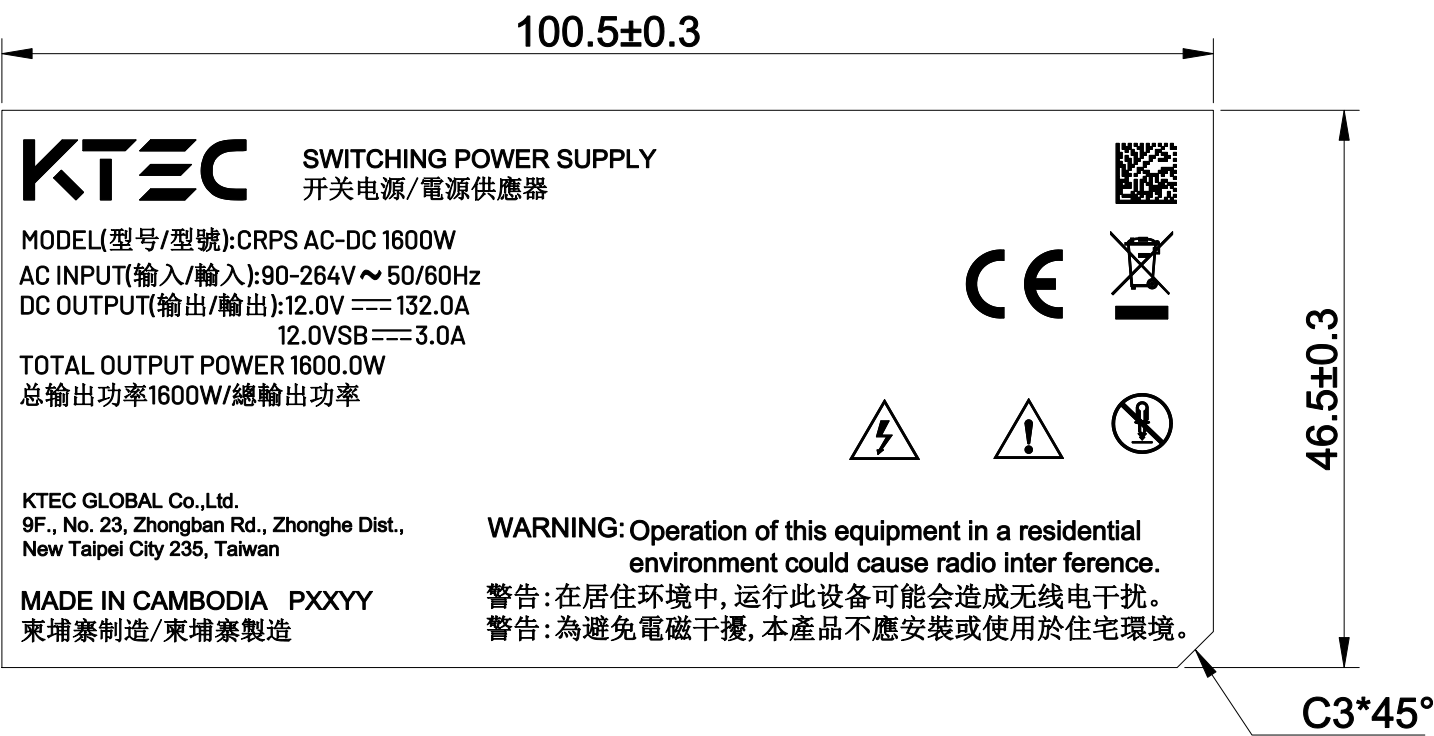
The leakage current at 264Vac/63Hz shall not be over 3.5mA RMS.

SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072

11. NAME PLATE



SWITCHING POWER SUPPLY

CRPS AC-DC 1600W

Manufacturer Part No.: KS260072



12. PACKING (UNIT: MM)

TBD