KTEC

SPECIFICATION FOR APPROVAL

CRPS AC-DC 300W

SWITCHING POWER SUPPLY

SWITCHING POWER SUPPLY

CRPS AC-DC 300W Manufacturer Part No.: KE260018

Customer Name_____

Customer Part NO. _____

Project Modify List

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1	First REV.	A	2026-01-19	Liao Xiaoyan	Edy Sung

Manufacturer

SALES	QE	APPROVED BY	MADE BY
Bryant	徐海鑫	贺洪明	冯朵朵

Approved Signatures

APPROVED BY	CHECKED BY	TESTED BY

SWITCHING POWER SUPPLY

CRPS AC-DC 300W Manufacturer Part No.: KE260018

9F., No. 23, Zhongban Rd., Zhonghe Dist., New Taipei City 235024 , Taiwan (R.O.C.)
+886-2-2223-3518 | sales@twktec.com.tw

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1. General

This specification defines the functional requirements of the switching power supply. It is a redundant server power supply with features support hot plug N+M (N=2 max, M=2 max), dual outputs (+12Vand +12VSB), AC input auto ranging with power factor corrected, and internal fan(s) for force air cooling. Complies with Europe RoHS2.0 required.

2. Mechanical overview

The physical size of the power supply enclosure is 40mm x 73.5mm x 185mm.The power supply contains a single 40mm fan. The power supply has a card edge output that interfaces with 2*25 card edge connector in the system. The AC plugs directly into the external face of the power supply. Refer to the following Figure 1 for All dimensions are nominal.

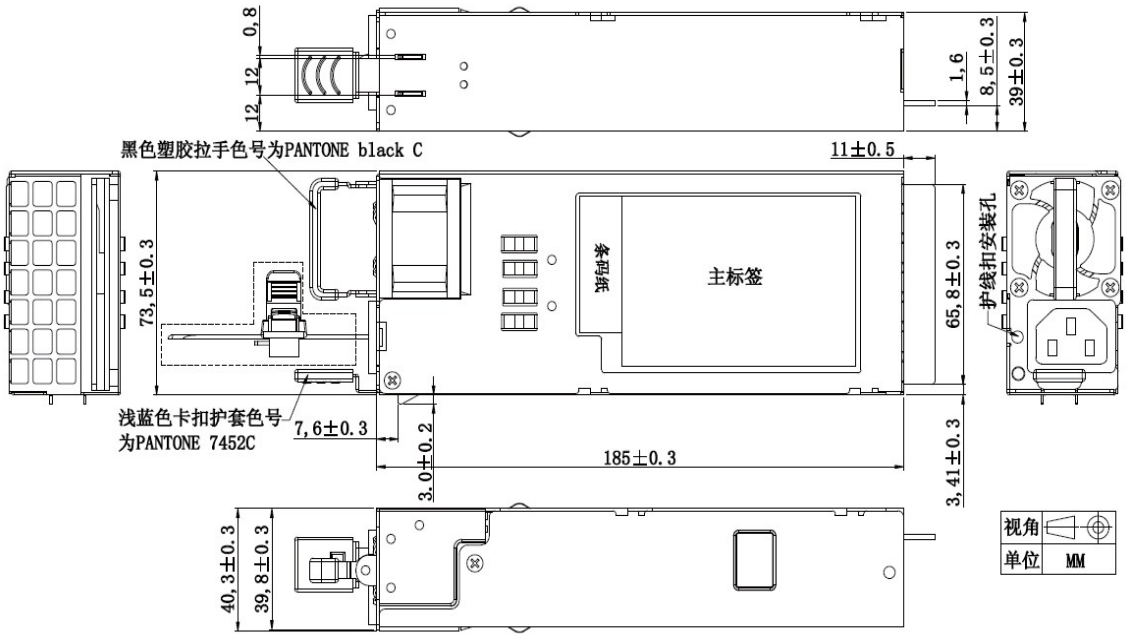


Figure 1 Power Supply Outline Drawing

2.1 DC Output Connector

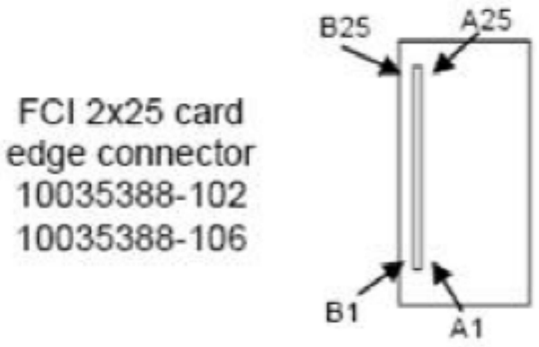
The power supply shall use a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector.

Table. DC Output Connector

Pin-out	Definition	Pin-out	Definition
A1-9	GND	B1-9	GND
A10-18	+12V	B10-18	+12V
A19	PMBus SDA	B19	A0 (SMBus address)
A20	PMBus SCL	B20	A1 (SMBus address)
A21	PSON	B21	+12V Stby
A22	SMBALERT #	B22	SMART_ON
A23	Return Sense(Remote Sense-)	B23	+12V load share bus
A24	+12Vremote Sense((Remote Sense+)	B24	PRESENT#(Reserved)
A25	PWOK	B25	NC

Table 1 DC Output Connector Pinout

Note: B25 is optional signal for PS_KILL or Vin_good;



Back DC output golden finger port

2.2 Handle retention

The power supply has a handle to assist extraction. The module can be able to be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.

The handle protects the operator from any burn hazard through the use of the Customer Corporation Industrial designed plastic handle.

2.3 Led marking and identification

The power supply has a single bi-colored LED for indication of the power supply status. Green &Amber. Below are table showing the LED states for each power supply operating state.

Power Supply Condition	LED State
Output ON and OK	GREEN

No DCIN power to all power supplies	OFF
DCIN present / Only 12VSB on (PS off) or PS in Smart on state	1Hz Blink GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	RED
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink RED
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER
Power supply FW updating	2Hz Blink GREEN

2.4 Airflow direction

The airflow direction shall be from the AC inlet side of the power supply to the card edge connector side (Fan in & reverse Fan).

2.5 Acoustic requirements

The power supply incorporates variable speed fan(s). The declared sound power levels (LwAd) of the power supply meet the requirements shown in the table. Sound power will be measured according to ECMA 74 (www.ecma-international.org) and reported according to ISO 9296.

Table2. Sound Power Requirement

Acoustic Operating Condition	% of Maximum Loading Condition	Altitude	Ambient(Inlet Temperature Condition)	LWA (dBA)
Idle	20%	900m	35°C	TBD
Operating	60%	900m	40°C	TBD
Performance	100%	900m	50°C	TBD

2.6 Temperature requirements

Table: Environmental Requirements

Description	Min	Max
Operating temperature range	0°C	55°C
Non-operating temperature range	-40°C	70°C

3. AC input requirements

3.1 Power factor

The power supply have greater the power factor requirements stated in the Energy Star® Program Requirements for Computer Servers. Power factor specification as below.

Output power	10% load	20% load	50% load	100% load
Power factor	NC	> 0.90	>0.96	>0.98
Input conditions	230Vac/50Hz and 115Vac/60Hz.			

3.1.1 Ithd

The below table shown the power supply “Total Harmonic Distortion” limits which according EN61000-3-2 standard:

Output power	≥20%	≥50%	≥100%
Current iTHD	≤20%	≤ 10%	≤ 8%
Input conditions	115VAC/230VAC & 50Hz / 60Hz		

3.2 AC inlet connector

The AC input connector shall be an IEC 320 C-14 power inlet. This inlet is rated for 10A / 250VAC.

3.3 AC/DC input voltage specification

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a blown fuse. The voltage level between shutdown and recovery shall have a minimum of 5 VAC/HVDC of voltage hysteresis, so that the power supply will not oscillate on and off due to voltage change condition.

AC/DC input voltage range

PARAMETER	MIN	RATED	VMAX	Start Up VAC	Power Off VAC
AC Voltage range	90 Vrms	100-240Vrms	264Vrms	85VAC ±5VAC	75VAC ±5VAC
Frequency	47 Hz	50/60	63 Hz	NA	NA
HVDC (240V)	180	240	300	170VDC±5VDC	160VDC±5VDC

Note: The Brown IN/OUT Hysteresis min is 5Vac

1. Maximum input current at low input voltage range is measured at 100-127Vac, at max load. (5.0Arms);

2. Maximum input current at high input voltage range is measured at 200-240Vac, at max load. (2.5Arms);
3. 2.5Arms maximum while input voltage is 240VDC.at max load;
4. AC Brown-in/out loading is 80%load; (low line & high line)

3.4 AC line isolation requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, power supply vendor provide Customer with written confirmation of dielectric withstand test which includes voltage level, duration of test and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully.

Transformers isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used.

In addition the insulation system must comply with reinforced insulation per safety standard IEC 62368-1. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 62368-1 spacing requirements.

3.5 AC line dropout / holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements.

The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Loading	Hold up time
100%	10msec

Note: This test condition loading is 100% of max loading.

3.5.1 AC line 12VSB holdup

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de- asserted).

3.6 AC line fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a slow blow type.

AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.7 AC inrush

AC line inrush current shall not exceed 50A peak, for up to one-quarter of the AC cycle, after which the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top). Inrush current caused by x- or y-caps is not considered.

3.8 AC line transient specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply is required to meet Performance Criterion A with the exception of IEC61000-4-11 Voltage Interruptions (>95% reduction 250 periods) where the power supply is required to meet Performance Criterion C.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Ac line sag transient performance

AC Line Sag (10sec interval between each sagging)				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC	95%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance.
> 1 AC cycle	>30 %	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable

Ac line surge transient performance

AC Line Surge				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage	50/60Hz	No loss of function or performance.
0 to ½ AC cycle	30 %	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

3.9 Susceptibility requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS power supply specification.

For further information on Customer standards please request a copy of the Customer Environmental Standards Handbook.

Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.10 Electrostatic discharge susceptibility

The power supply shall comply with the limits defined in EN 55035 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.15KV air discharge,8KV Contact discharge, performance criteria A.

3.11 Fast transient/burst

The power supply shall comply with the limits defined in EN55035 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR24.

3.12 Radiated immunity

The power supply shall comply with the limits defined in EN55035 using the IEC61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24.

3.13 Surge immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55035, EN 61000-4-5: Edition 1.1:2001-04.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition. The power supply shall comply with the limits defined in EN55035 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria A defined in Annex B of CISPR 24.

3.14 Power frequency magnetic immunity

The power supply shall comply with the limits defined in EN55035 using the IEC61000-4-8:2009 Power Frequency Magnetic Field Immunity Test standard.

3.15 Power recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

4 Efficiency

The following table provides the required minimum efficiency level at various loading conditions at 25 degrees condition stated. These are provided at different load levels; 100%, 50%, 20% . Output shall be load according to the proportional loading method defined by 80 Plus Gold in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7. The fan losses are not included in the efficiency calculation and measurements.

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
230Vac/60Hz	89%	92%	88%	NC

Efficiency requirement

5 DC output specification

5.1 Main output power / currents

The following tables define the power and current ratings. The power supply must meet both static and Dynamic voltage regulation requirements for all conditions.

Table：Output load ratings

Parameter	+12V Output
Output Voltage	+12VDC Notes 1
Minimum Current	0A
Maximum Current	2.1A
Line Regulation	+/-5%
Load Regulation	+/-5%
Overshoot	5%
Undershoot	5%

Notes：

1) Output voltage adjusted to 12Vdc+/-0.05Vdc @50% load

The following tables are defines the PSU type’ s peak loading requirement

Table：CRPS Load Requirements

Output	Input Voltage (VAC)	Min (A)	Max. Continuous (A)	CLST Peak 20sec duration 2(A)	Pmax.app Peak 10msec duration 3(A)
12V Main	100-240	0.0	PSU rating(25A)	Rated + 5A	Rated + 25A
12Vstby 1	100-240	0.0	2.1	N/A	N/A

5.2 12VSB output

12VSB is a standby supply output that is active whenever the AC power is present. This output provides a power source for circuits that must remain operational when the main DC outputs are in a disabled state.

Parameter	+12V sb
Voltage	+12VDC
Minimum Current	0A
Maximum Current	2.1A
Line Regulation	+/-5%
Load Regulation	+/-5%
Overshoot	5%
Undershoot	5%

5.3 Voltage regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise.These shall be measured at the output connectors.

Voltage Regulation Limits

PARAMETER	TOLERANCE	MIN	NOM	MAX	UNITS
+12V	- 5% / +5%	+11.4	+12	+12.6	Vrms
+12Vstby	- 5% / +5%	+11.4	+12	+12.6	Vrms

5.4 Dynamic loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the tables below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The △ step load may occur anywhere within the MIN load to the MAX load conditions.

Transient load requirements

Output	Δ Step Load Size (See note)	Load Slew Rate	Test capacitive Load
+12V	50% of Load Max	0.5 A/μs	2200μF
+12VSB	1.0A	0.5 A/μs	1000μF

Note: For dynamic condition +12V min loading is 1A

5.5 Capacitive loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Capacitive loading conditions

Output	MIN	MAX	Units
+12V	2200	20000	uF
+12VSB	100	3100	uF

5.6 Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 0.1Ω. This path may be used to carry DC current.

5.7 Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in contents 5.5 stable. A minimum of: 45 degrees phase margin and -10dB gain margin is required. The power supply manufacturer shall provide proof of the unit’ s closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

5.8 Residual voltage immunity in standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from Standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on. The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PS_ON signal is de-asserted.

5.9 Common mode noise

The Common Mode noise on any output shall not exceed 350mV PK-PK over the frequency band of 10Hz to 20MHz. The measurement shall be made across a100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure). The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.10 Soft starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

5.11 Zero load stability requirements

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.12 Hot swap requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

5.13 Forced load sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations.

The VLs(12V load share bus) pin shell be connected together at user system board for load sharing function of two units.all the remote sense pins of power supplies must to be placed at the same point on +12V and its return path at system side.

The +12VSB output is passive current sharing between power supplies (without active sharing). The +12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause the output to go out of regulation in the system.

The % of current share error is defined as follows for 1+1 power supplies:

%Error = 100 x |PS1 current – PS2 Current| / (PS1 current + PS2 Current)

Note: In paralleling mode, the system loading shall be gradually increased to the specified max. rating. It should not greater than one single PSU' s max. loading before PWOK asserted during turn on period and the following step loading (include start-up, AC-off and hot- swap).

NOTES: Current sharing has to meet following accuracy at different load range running in 1+1 configuration.

5.14 Ripple / noise

The maximum allowed ripple/noise output of the power supply measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor is placed at the point of measurement. To help reduce switching ripple further, an additional 1000uF low ESR electrolytic capacitor may be placed in parallel(or add minimum capacitive loading of each output also).

Ripples and Noise

+12V main	+12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below.

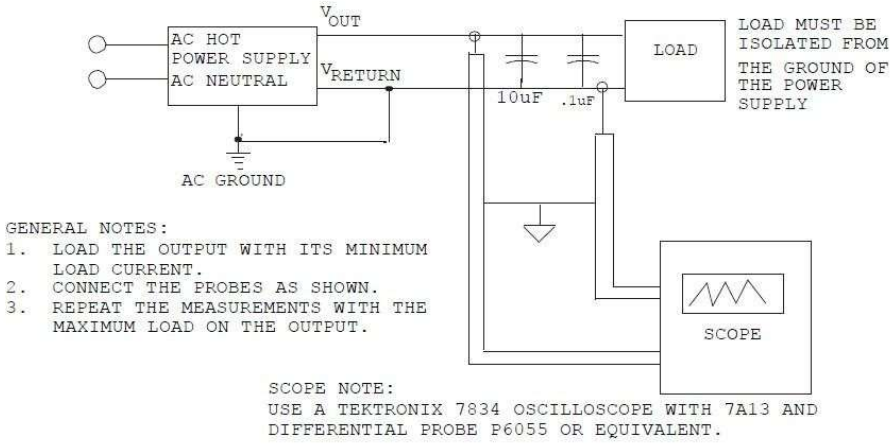


Figure 2 Differential Noise test setup

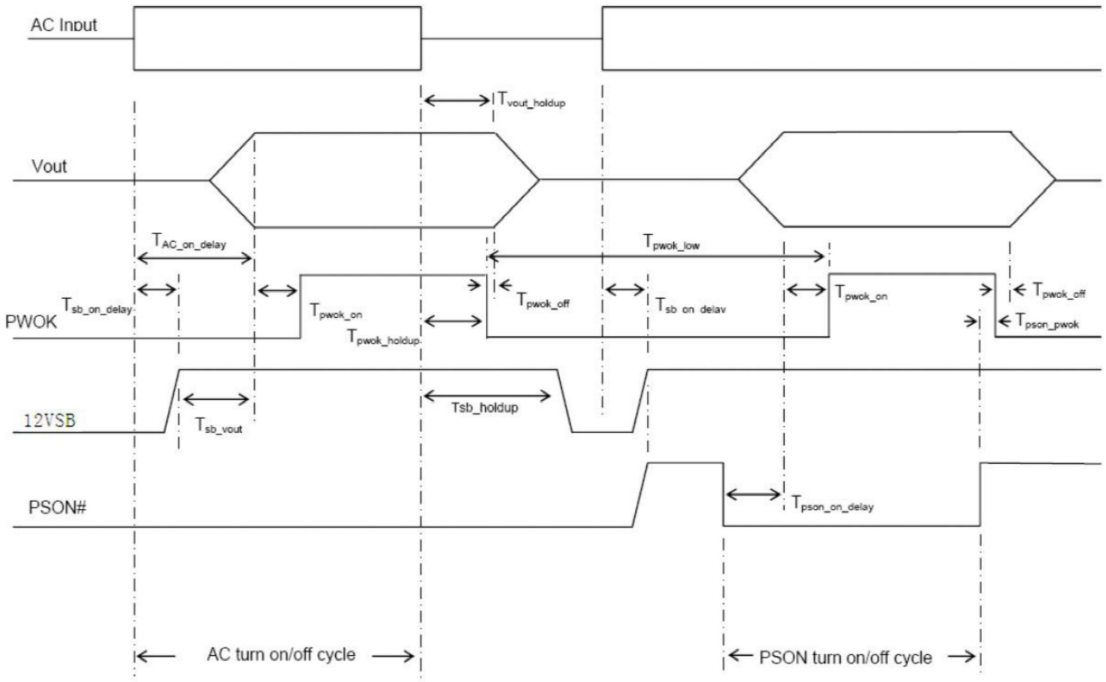
Note: When performing this test, the probe clips and capacitors should be located close to the load.

5.15 Timing requirements

Timing value :

ITEM	DESCRIPTION	MIN	MAX	UNITS
TV out rise	Output voltage rise time from each main output.	1	50	ms
T12VSB rise	Output voltage rise time for the +12VSB output.	1	50	ms
Tsb-on delay	Delay from AC being applied to 12VSB being within regulation.		1500	ms
Tsb-on delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
TV out holdup	Time 12V output voltage dropping to regulation after loss of AC at 100% load condition	11		ms
TPWOK holdup	Delay from loss of AC to desertion of PWOK at 100% load condition.	10		ms
Tpson_on_delay	Delay from PSON#active to output voltages within regulation limits.	5	400	ms
Tpson PWOK	Delay from PSON# deactivate to PWOK being deserted.			ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok off	Delay from PWOK de-asserted to +12V dropping out of regulation limits.	1		ms
Tpwok_low	Duration of PWOK being in the deserted state during an off/on cycle using AC or the PSON# signal.	100		ms
Tsb_vout	Delay from 12 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T12VSB holdup	Time the +12VSB output voltage stays within regulation after loss of AC.	70		ms

Signal Timing Sequence 1:



6 Protection circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an DC OFF for 15sec and a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

6.1 Current limit (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

OCP and OCW Requirements for CRPS-185

Spec	Description	MI	MA	MIN	MAX
Slow OCP	Slow over current protection (shutdown and latch after MIN/MAX timing)	Rating + 10A	Rating + 18A	20msec	200msec
Slow OCW	Slow over current warning (SMBALERT#)	Rating + 6A	Rating + 10A	10msec	15 msec
OCPstby	Stby over current protection (shutdown, hiccup mode) (shutdown, hiccup mode)	3.5A	4.5A	1msec	100msec

6.2 Over voltage protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply' s connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSB will be auto-recovered after removing OVP limit.

Output	Action voltage			Units
	Min	Nom	Max	
+12VSB	13.3	14.0	14.5	V
+12V	13.3	14.0	14.5	V

6.3 Over temperature protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall have a minimum of 5℃ of ambient temperature margin.

6.4 Short circuit protection (SCP)

The power supply shall shut down and latch off for shorting the main outputs. 12VSB must be capable of being shorted indefinitely. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing SCP limit.

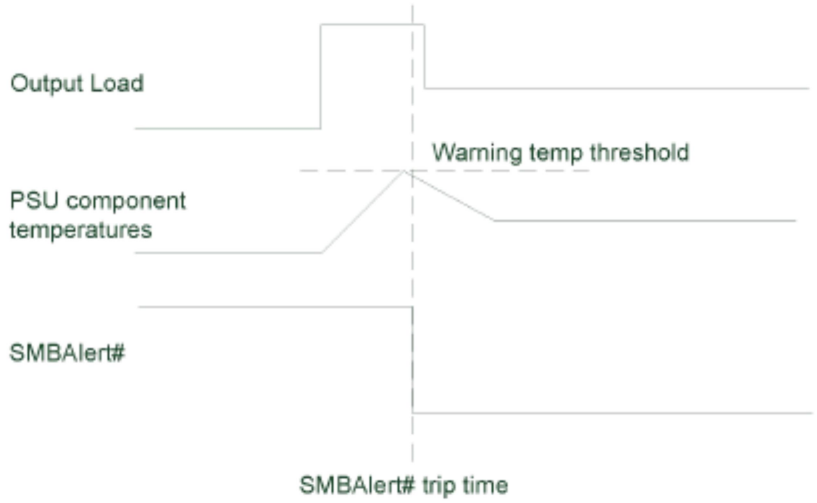
6.5 Over power protection (OPP)

The power supply shall support over power protection (OPP) level low enough to protect the power supply running in this mode for repeated 1msec durations at a 1% duty cycle. The power supply shall be stable operating at any load point from rated power up to the OPP point.

6.6 Closed loop system throttling(CLST)

The power supply will always assert the SMBALERT# signal whenever temperature-monitored component in the power supply reaches a warning threshold. Upon reduction of the load within 2msec after the SMBALERT# signal is asserted if the load is reduced to less than the power supply rating; the power supply will continue to operate and not shutdown.

Figure CLST Timing Requirements



6.7 Smart ride-through(SMART)

The power supply will assert the SMBALERT# signal < 4msec after AC input voltage is lost to 0Vac.

7 Control and indicator functions

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true.

7.1 Device address location (B19: A0; B20: A1)

Address Bit 0: A 10kΩ pull-up resistor pulled to internal +3.3V in the PSU.

Address Bit 1: A 10kΩ pull-up resistor pulled to internal +3.3V in the PSU.

Locations	PSU#1	PSU#2
PBD addressA1/A0	0/0	0/1
Power supply FRU device	A0h	A2h
Power supply PSMI device	B0h	B2h
Signal type	10k ohm pull up resistor from +3.3Vdd device.	
A1 or A0=low	A1 or A0 address bit=0	
A1 or A0=high	A1 or A0 address bit=1	
	Minimum	Maximum
Logic level low voltage	0V	0.4V
Logic level low voltage	2.4V	3.46V

7.2 I2C BUS (A20: SCL; A19: SDA)

Each module shall provide SCL/SDA bus for EEPROM read/write of system. It's pull up from +3.3Vdd device by a 10K ohm resistor. System should be has 1k~2k ohm pull high resistor on the SCL/SDA bus. SCL/SDA pin should be link together and closer. The SCL/SDA bus total capacitance must be lower 100pF from system and PDB. The max I2C bus speed is 100kHz and the MCU of PSU is slave device in I2C bus. The time interval of I2C command is 1ms.

7.3 SMBALERT# indicate(Pin A22: SMBALERT#)

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

Signal Type (Active Low)	Open collector / drain output from power supply. Pull-up to 3.3VSB located in power supply.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50uA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 uA

7.4 PS-ON input signal (pinA21: PS-ON)

The PS-ON signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn

off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Signal Type	Accepts an open collector/drain input from the system. Pull-up to 3.3VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4mA
Power off delay: Tpson_off_delay		5msec
Power up delay: Tpson_on_delay	5msec	400msec
PWOK delay: T pson_PWOK		5msec

7.5 PWOK output signal (PIN A25: PWOK)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when DC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See Table: for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Signal Type	Open collector/drain output from power supply. Pull-up to 3.3VSB located in the power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
Power supply PSMI device	MIN	MAX
Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200 A	2.4V	3.46V
Sink current, PWOK = low		400uA
Source current, PWOK = high		2mA
PWOK delay: Tpwok_on	100ms	500ms
PWOK rise and fall time		100 sec

7.6 Smart on control (PIN B22: enable by system)

Before enabling Smart On function, make sure pin B22 (SMART ON) on output golden finger of each PSU is connected together. When the pin is HIGH in the Smart On mode, the slave power supply will enter the Smart

Standby mode if system total loading under PSU's pre-set load level. When the pin is LOW in the Smart On mode, the Smart Standby mode power supplies will work in normal redundancy mode.

Smart On feature supports 1+1, 2+1, and 3+1 redundant configurations. It uses the PMBus manufacturer specific command area to define PMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to Smart On. We will call the command SMART_ON_CONFIG (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

Cold_Redundancy_Config (D0h)		
Value	**State**	**Description**
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply make sure no other PSU enter Smart_On mode.
01h	Cold Redundant Active 1	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1 1	Defines the power supply that is third to turn off in a Smart On configuration (500ms later) and first to turn on as the load increases.
03h	Cold Standby 2 1	Defines the power supply that is second to turn off in a Smart On configuration (600ms later) and second to turn on as the load increases.
04h	Cold Standby 3 1	Defines the power supply that is first to turn off in a Smart On configuration (400ms later) and third to turn on as the load increases.

The trigger levels above may have a +/-10% tolerance for actual application. The default state of power supply is in Standard Redundancy mode. Power supply need to be re-specified a state whenever initial power on or the operating module predicts failure. The SMART_ON_CONFIG command will reset to 00h (Standard Redundancy) when any fault happened. And when an active power supply asserts, all parallel power supplies in Smart Standby mode shall power on immediately.

7.6.1 Smart standby power supply operating state

A power supply is put into Smart Standby whenever PSON# is asserted, SMART_RED# is de-asserted, and SMART_ON_CONFIG value is set to 02h, 03h, or 04h. In the Smart Standby mode the power supply must.

1) Power ON when Smart_On bus is driven LOW.
2) Keep PWOK asserted.
3) No PMBus fault conditions reported via STATUS commands, any fault happen will made PSU leave smart standby mode.
4) keep all fans rolling

5) LED is green blinking under normal conditions, amber blinking if any warning conditions happen.

7.6.2 Powering on smart standby supplies to maintain best efficiency

Power supplies in Smart Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the Smart Standby configuration; will slightly change the load share threshold that the power supply shall power on at.

7.6.3 Powering on smart standby supplies during a fault or over current condition

Some warnings happen or 12V output shutdown due to any fault will cause SRED_OK# driven low. When an active power supply asserts its SRED_OK# signal, all parallel power supplies in Smart Standby mode shall power on immediately.

The trigger condition:

1) 12V OC warning/ fault happens

2) 12V OVP fault

3) 12V Smart ON UVP (lower than 11.8V)

4) OTP fault

5) fan speed fault

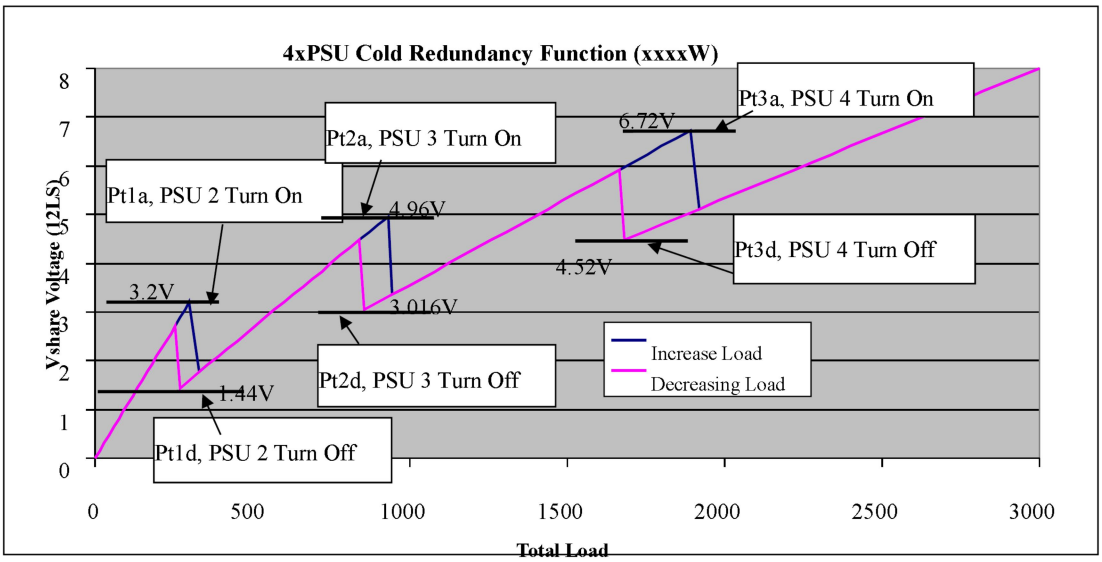
6) DC loss

7) send 00h to PMBus D0h command

8) PSON# de-assertion happen

7.6.4 The way to enable Smart On function

Here are the steps to put PSU into smart on mode. PSU which is assigned as smart on standby can operate in a power-off state and turn on main power if necessary.



Power On/Off of power supplies in Smart On Mode (4xxxxW PSUs)

7.7 Present_N# (Pin B24, Optional)

This signal is an active low type signal and is connected to the power supply's output ground internally. The mating pin of this signal in system side should have a pull-up resistor which limit the max. current 4mA to go through from this signal pin to the power supply. A Low state on this signal indicates the PSU is physically presents.

7.8 VIN_Good (Pin B25, Optional)

The purpose of the PS_KILL pin is to enhance for hot swapping of the power supply. The PS_KILL pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PS_KILL pin will quickly turn off the power supply main output +12V and prevent arcing of the DC output contacts. When the PS_KILL signal pin is not pulled down or left opened (power supply is extracting from the system), the power supply shuts down regardless of the condition of the PSON# signal. The mating pin of this signal in the system should be tied to ground.

Internal to the power supply, the PS_KILL pin is connected to an internal +3.3V voltage through a 10k pull-up resistor. Upon receiving a LOW state signal at the PS_KILL pin, the power supply will be allowed to turn on via the PSON# signal. A LOW state on this pin by itself will not turn on the power supply +12V output. Below table shown the PS_KILL signal characteristics.

Table PS_KILL Signal Characteristics

Signal States	+12V
_KILL = LOW, PSON = LOW	ON
PS_KILL = HIGH or OPEN, PSON = LOW	OFF
PS_KILL = LOW, PSON = HIGH or OPEN	OFF

8 Environmental requirements

8.1 Temperature

Operating Ambient: 0℃ to +55℃

Non-operating Ambient: -40℃ to +70℃

8.2 Humidity

Operating:5% to 85% relative humidity (non-condensing)

Non-Operating: 5% to 95% relative humidity (non-condensing)

8.3 Altitude

Operating: To 5000 m;The PUS shall support rated load at 950 m with Max. operating ambient, once the altitude is over 950m, the ambient de-rating is -1°C /125 m.

Non-operating: To 15200 m;

8.4 Mechanical shock

Non-operating: 50 G Trapezoidal Wave, Velocity change = 170 in. / sec.

Three drops in each of six directions are applied to each of the samples.

8.5 Random vibration

Non-Operating Test

Sinusoidal: Input Acceleration: 1.5G, peak to

peak Frequency Band: 10Hz-500Hz-10Hz

Sweep Rate: 0.5 Octaves/minute

Sweep Time: Two sweeps per axis

Orientation: Three mutually perpendicular axes

Random: Break Point: 2Grms, 10Hz-500Hz frequency content

Dwell Time: 60 minutes per axis

Orientation: Three mutually perpendicular axes

8.6 Thermal shock (shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30℃/min. ≧ transition time ≧ 15℃/min.

duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

8.7 Audible noise

Maximum audible noise allowed <70dB at 100% rated DC load at 25 degree Celsius ambient inlet air temperature(Noise test sensor the distance from the fan 1m).

9 FRU requirements

9.1 Overview

The PMBus features included in this specification are requirements for ac/dc golden box power supply for use in server systems. This specification is based on the PMBus™ specifications parts I and II, revision 1.2.

9.2 Related Documents

PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2.

PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2. SMBus 2.0.

9.3 Hardware Connecting

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the or'ing device. The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

Only weak pull-up resistors shall be on SCL or SDA inside the power supply. The main pull-up resistors are provided by the system and may be connected to 3.3VSB. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

.300ns maximum fall time with a 400pF capacitive load and 2.7Kohm pull up to 3.3V

.10ns minimum fall time with a 20pF capacitive load and 2.7Kohm pull up to 3.3V

.The power supply shall not load the SMBus if it has no input power

9.4 Data Speed

The PMBUS device in the power supply shall operate at the full 100 kbps SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching.

The PMBus device shall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

9.5 Bus Error

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the

SMBus specification. The device is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

9.6 FRU Data Format

For identification of the power supply an internal 256x8 bit EEPROM with PMBus interface is used. The information in the EEPROM follows the IPMI (Platform Management FRU Information Storage Definition) guidelines Document Revision 1.1 from November 15, 1999.

9.7 Communication Address

Four pins will be allocated for the FRU and PMBus information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines A0-A1 to indicate to the power supply's EEPROM and MCU. which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

A1 Logical voltage	A0 Logical voltage	PSU address	FRU address
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

10 PMBus Content

10.1 PMBus Command Table

Via the PMBus the computer system can communicate with the power supply to access currents, voltages, fan control and speed and temperatures. The communication follows the Power System Management Protocol Specification. (PMBus 1.2). As soon as AC Power is connected to the PSU the PMBus functionality must be available.

Following table shows mandatory PMBus commands to be supported by the PSU.

Table 10.1. Supported PMBus Command

Command Code	Command Name	SMBus Transaction Type:		Number Of Data Bytes	Comment
		Writing Data	Reading Data		
00h	PAGE	Write Byte	Read Byte	1	
01h	OPERATION	Write Byte	Read Byte	1	0x80 ON; 0x00 OFF Default: 0x00
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	
03h	CLEAR_FAULTS	Send Byte	N/A	0	
05h	PAGE_PLUS_WRITE	Block Write	N/A	Variable	
06h	PAGE_PLUS_READ	N/A	Block Write – Block Read	Variable	
19h	CAPABILITY	N/A	Read Byte	1	0xB0
1Ah	QUERY	N/A	Block Write – Block Read	1	
1Bh	SMBALERT_MASK	Write Word	Block Write – Block Read	2	
20h	VOUT_MODE		Read Byte	1	0x17 (n=-9)
21h	VOUT_COMMAND	Write Word	Read Word	2	
30h	COEFFICIENTS	N/A	Block Write – Block Read	5	Use for Ein/Eout
31h	POUT_MAX	N/A	Read Word	2	
3Ah	FAN_CONFIG_1_2	Write Byte	Read Byte	1	
3Bh	FAN_COMMAND_1	Write Word	Read Word	2	
4Ah	IOUT_OC_WARN_LIMIT		Read Word	2	
51h	OT_WARN_LIMIT		Read Word	2	
5Dh	IIN_OC_WARN_LIMIT		Read Word	2	
6Ah	POUT_OP_WARN_LIMIT		Read Word	2	
6Bh	PIN_OP_WARN_LIMIT		Read Word	2	
78h	STATUS_BYTE	Write Byte	Read Byte	1	
Bit 6	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC				
Bit 3	VIN_UV				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
79h	STATUS_WORD	Write Word	Read Word	2	
Bit 7(H)	VOUT				
Bit 6	IOUT/POUT				
Bit 5	INPUT				
Bit 3	POWER_GOOD#				
Bit 2	FANS				
Bit 6(L)	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC_FAULT				

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Bit 3	VIN_UV_FAULT				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
7Ah	STATUS_VOUT	Write Byte	Read Byte	1	
Bit 7	VOUT_OV_FAULT				
Bit 4	VOUT_UV_FAULT				
7Bh	STATUS_IOUT	Write Byte	Read Byte	1	
Bit 7	Iout OC fault				
Bit 5	Iout OC warning				
Bit 1	Pout OP fault				
Bit 0	Pout OP warning				
7Ch	STATUS_INPUT	Write Byte	Read Byte	1	
Bit 5	Vin UV warning				
Bit 4	Vin UV fault				
Bit 3	Unit off for insufficient input				
Bit 1	Iin over current warning				
Bit 0	Pin over power warning				
7Dh	STATUS_TEMPERATURE	Write Byte	Read Byte	1	
Bit 7	OT fault				
Bit 6	OT warning				
7Eh	STATUS_CML	Write Byte	Read Byte	1	
Bit 7	Invalid COMMAND				
Bit 6	Invalid DATA				
Bit 5	PEC Failed				
81h	STATUS_FANS_1_2	Write Byte	Read Byte	1	
Bit 7	Fan 1 fault				
Bit 5	Fan 1 warning				
Bit 3	Fan1 speed overridden				
86h	READ_EIN	N/A	Block Read	6	DIRECT Data Format
87h	READ_EOUT	N/A	Block Read	6	DIRECT Data Format
88h	READ_VIN	N/A	Read Word	2	Linear
89h	READ_IIN	N/A	Read Word	2	Linear
8Bh	READ_VOUT	N/A	Read Word	2	Linear16
8Ch	READ_IOUT	N/A	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1	N/A	Read Word	2	Ambient
8Eh	READ_TEMPERATURE_2	N/A	Read Word	2	SR Hotspot
8Fh	READ_TEMPERATURE_3	N/A	Read Word	2	PFC Hotspot
90h	READ_FAN_SPEED_1	N/A	Read Word	2	In RPM
96h	READ_POUT	N/A	Read Word	2	Linear
97h	READ_PIN	N/A	Read Word	2	Linear
98h	PMBUS_REVISION	N/A	Read Byte	1	1.3
99h	MFR_ID	Block Write	Block Read	Variable (8)	"SEGOTEP"
9Ah	MFR_MODEL	Block Write	Block Read	Variable (13)	"XXXXXXXXXXXX"
9Bh	MFR_REVISION	Block Write	Block Read	Variable (3)	"RXX"
9Ch	MFR_LOCATION	Block Write	Block Read	Variable (5)	"CHINA"
9Dh	MFR_DATE	Block Write	Block Read	Variable (8)	"YYYYMMDD"

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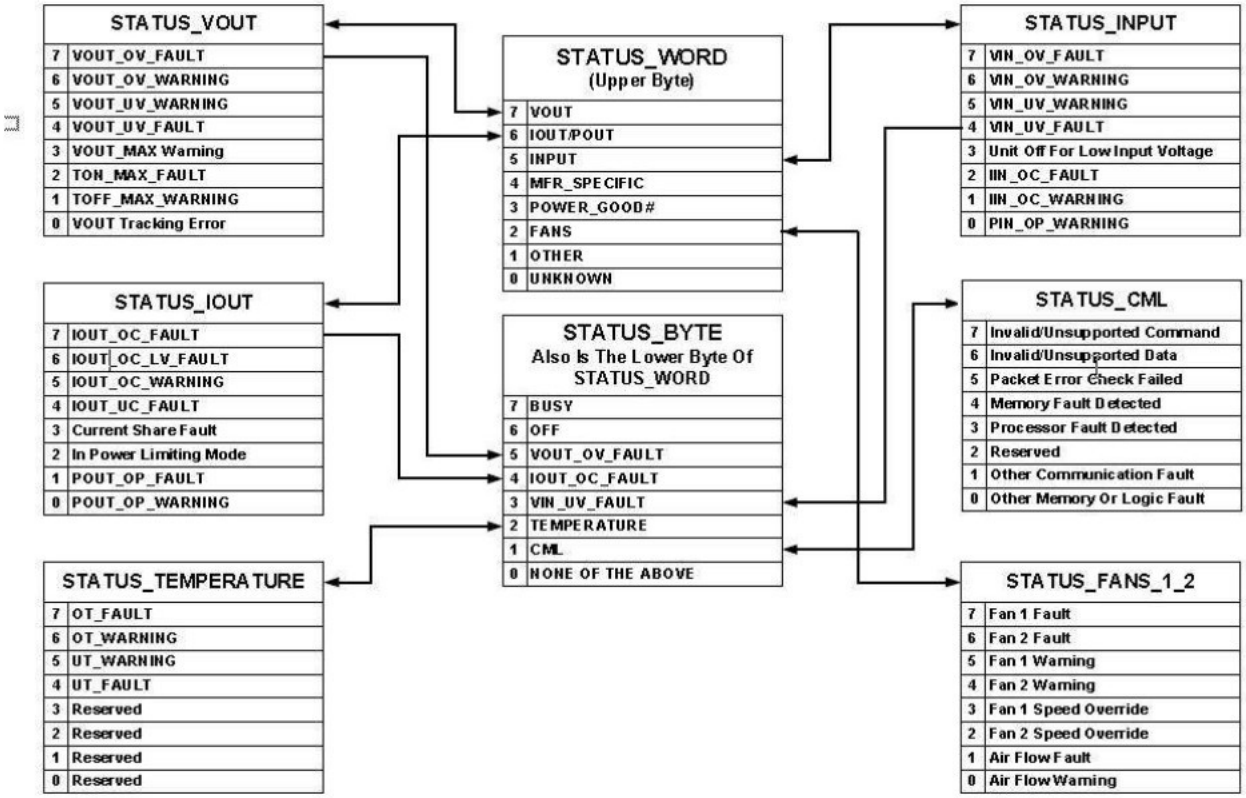
9Eh	MFR_SERIAL	Block Write	Block Read	Variable (19)	Serial Number
9Fh	APP_PROFILE_SUPPORT	N/A	Block Read	Variable (2)	PMBus 1.2
A0h	MFR_VIN_MIN	N/A	Read Word	2	90V
A1h	MFR_VIN_MAX	N/A	Read Word	2	264V
A2h	MFR_IIN_MAX	N/A	Read Word	2	
A3h	MFR_PIN_MAX	N/A	Read Word	2	
A4h	MFR_VOUT_MIN	N/A	Read Word	2	11.4V
A5h	MFR_VOUT_MAX	N/A	Read Word	2	12.6V
A6h	MFR_IOUT_MAX	N/A	Read Word	2	
A7h	MFR_POUT_MAX	N/A	Read Word	2	
A8h	MFR_TAMBIENT_MAX	N/A	Read Word	2	
A9h	MFR_TAMBIENT_MIN	N/A	Read Word	2	
AAh	MFR_EFFICIENCY_LL	N/A	Block Read	14	At 20%/50%/100%
ABh	MFR_EFFICIENCY_HL	N/A	Block Read	14	At 20%/50%/100%
B0h	PMBUS_MFR_ CALIBRATION_0xB0	Block Write	Block Read	Variable	
C0h	MFR_MAX_TEMP_1	N/A	Read Word	2	
C1h	MFR_MAX_TEMP_2	N/A	Read Word	2	
C2h	MFR_MAX_TEMP_3	N/A	Read Word	2	
D0h	MFR_COLD_ REDUNDANCY_CONFIG	Write Byte	Read Byte	1	
D4h	MFR_HW_COMPATIBILITY	N/A	Read Word	2	
D5h	MFR_FWUPLOAD_CAPABIL ITY	N/A	Read Byte	1	
D6h	MFR_FWUPLOAD_MODE	Write Byte	Read Byte	1	
D7h	MFR_FWUPLOAD	Block Write	N/A		
D8h	MFR_FWUPLOAD_STATUS	N/A	Read Word	21	
D9h	MFR_FW_REVISION	N/A	Block Read	3	
DCh	MFR_BLACK_BOX	N/A	Block Read	237	
DDh	MFR_REAL_TIME	Block Write	Block Read	4	
DEh	MFR_SYSTEM_BLACK_BOX	Block Write	Block Read	40	
DFh	MFR_BLACKBOX_CONFIG	Write Byte	Read Byte	1	
E0h	MFR_CLEAR_BLACKBOX	Send Byte	N/A	1	

10.2 Status commands

Figure 10.1. Summary Of The Status Registers



The following PMBus STATUS commands shall be supported. All STATUS commands stated in Table 7.1 Supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_ PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBALERT# signal. The new SMBALERT_MASK command is used to define which status event

Table 10.2. PMBus* STATUS Commands Summary

PMBus command	Bit location	PSU state when bit is asserted ('1')	Instances No PAGE'ing2 PAGE 00h = BMC PAGE 01h = ME	SMBALERT_MASK defaults for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBALERT# 1 = does not cause assertion of
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to		
CML	1 (lower)	ON		
VOUT	7 (upper)	Refer to STATUS_VOUT		
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		
INPUT	5 (upper)	Refer to STATUS_INPUT		
FANS	2 (upper)	Refer to STATUS_FANS		
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1,1,1
VOUT_UV_FAULT	4	OFF		1,1,1
STATUS_IOUT			No PAGE'ing, 00h,01h	
IOUT_OC_FAULT	7	OFF		1,1,0
IOUT_OC_WARNING	5	ON		1,1,0
POUT_OP_FAULT	1	OFF		1,1,1
POUT_OP_WARNING	0	ON		1,1,1
STATUS_INPUT			No PAGE'ing, 00h,01h	
VIN_UV_WARNING	5	ON		1,1,0
VIN_UV_FAULT 1	4	OFF		1,1,0
Unit off for low input voltage	3	OFF		1,1,1
IIN_OC_WARNING	1	ON		1,1,1

PIN_OP_WARNING	0	ON		1,1,1
STATUS_TEMPERATURE			No PAGE'ing, 00h,01h	
OT_FAULT	7	OFF		1,1,0
OT_WARNING	6	ON		1,1,0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault3	7	OFF		1,1,1
Fan 1 warning3	5	ON		1,1,1

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.

2 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.

3 All fans in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

10.3 PMBus Temperature Read Commands

The following temperature read commands as documented by the PMBus specification Part II version 1.2 should be supported.

READ_TEMPERATURE_1(8Dh), should provide the PSU inlet temperature.

READ_TEMPERATURE_2(8Eh), should provide the temperature of the SR heat sink in the PSU.

READ_TEMPERATURE_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

10.4 Page (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

10.5 Operation (01h)

The OPERATION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to turn the PMBus device output on and off.

Bit [7] controls whether the PMBus device output is on or off.

If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

10.6 ON_OFF_Config(02h)

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

The default response for any PMBus device is specified by the device manufacturer. The details of the ON_OFF_CONFIG data byte are shown in Table 14.1.

Example conditions:

If bit [4] is cleared, then the unit powers up and operates any time bias power is available regardless of the

setting of bits [3:0].

If bit [4] is set, bit [3] is set, and bit [2] is cleared, then the unit is turned on and off only by commands received over the serial bus.

If bit [4] is set, bit [3] is cleared, and bit [2] is set, then the unit is turned on and off only by the CONTROL pin.

If bit [4] is set, bit [3] is set, and bit [2] is set, then the unit is turned on and off only when both the commands received over the serial bus AND the CONTROL pin are commanding the device to be on. If either a command from the serial bus OR the CONTROL pin commands the unit to be off, the unit turns off.

Table 10.3. ON_OFF_CONFIG Data Byte

Bit Number	Purpose	Bit Value	Meaning
7:5	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	000	Reserved For Future Use
4		0	Unit powers up any time power is present regardless of state of the CONTROL pin
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)
		1	Active high (Pull high to start the unit)

0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay and fall Time
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device’s product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

10.7 Clear_faults Command (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

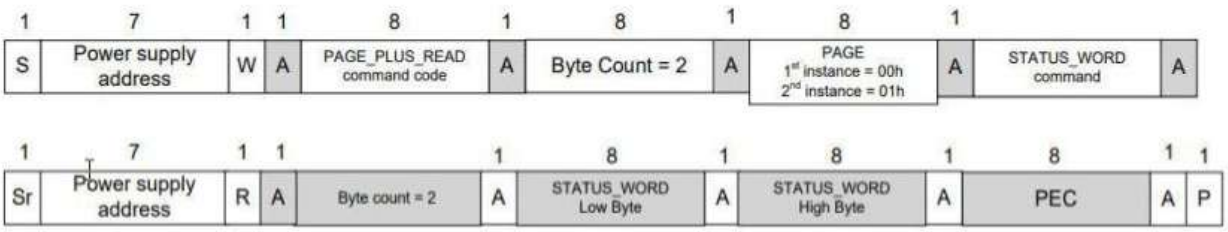
10.8 Page_plus_write / Page_plus_read commands (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_VOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Figure 10.2. Reading STATUS commands with PAGE_PLUS_READ

Reading STATUS_WORD

Block Write – Block Read Process Call with PEC



Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML

Block Write – Block Read Process Call with PEC

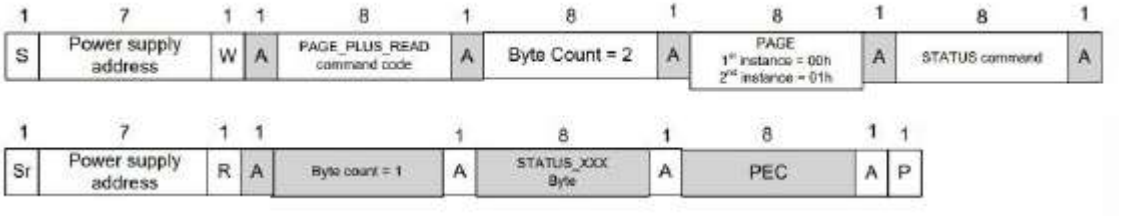
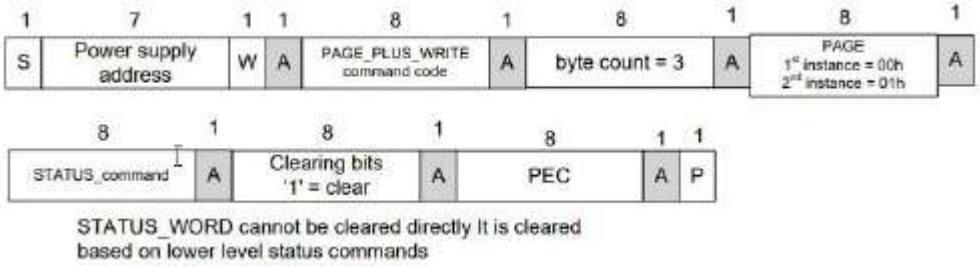


Figure 10.3. Clearing STATUS commands using PAGE_PLUS_WRITE

Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML

Block Write with PEC



10.9 Capability (19h)

This command provides a way for a host system to determine some key capabilities of a PMBus device. There is one data byte formatted as shown in Table 12.2. This command is read only.

Table 10.4 CAPABILITY COMMAND Data Byte Format

Bit Number	Purpose	Bit Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved

4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol
3:0	Reserved	X	Reserved

10.10 Query (1Ah)

The QUERY command is used to ask a PMBus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification

Table 10.5. QUERY Command Returned Data Byte Format

Bits	Value	Meaning
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	XX	Reserved for future use

If bit [7] is zero, then the rest of the bits are “don’ t care”.

10.11 SMBALERT_mask (1Bh)

This allows the system to mask events from asserting the SMBALERT# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBALERT# by writing a '1' to the associated STATUS bits. The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

Figure 10.4. PAGE_PLUS_READ command.

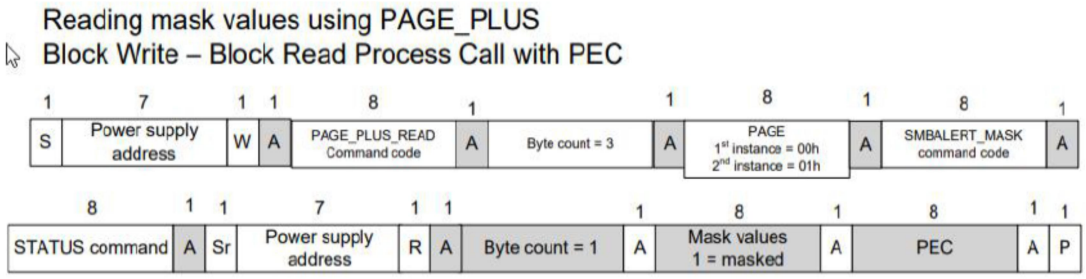
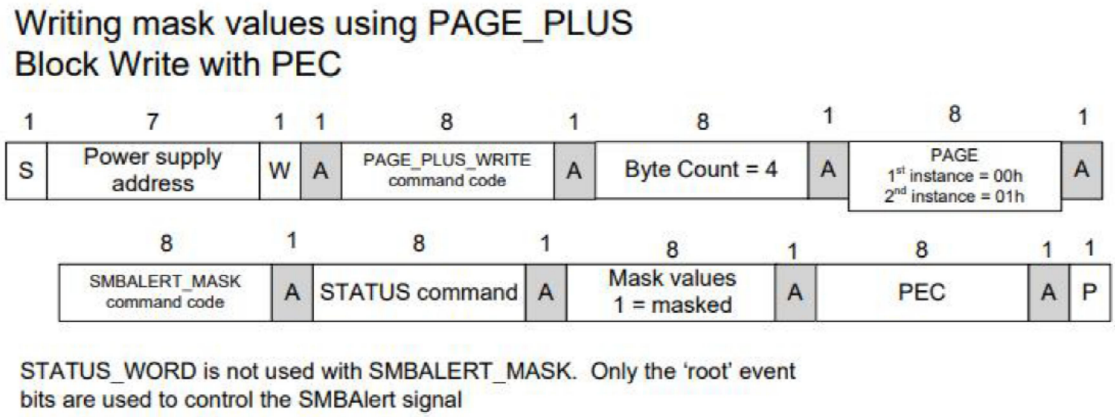


Figure 10.5. PAGE_PLUS_WRITE command.

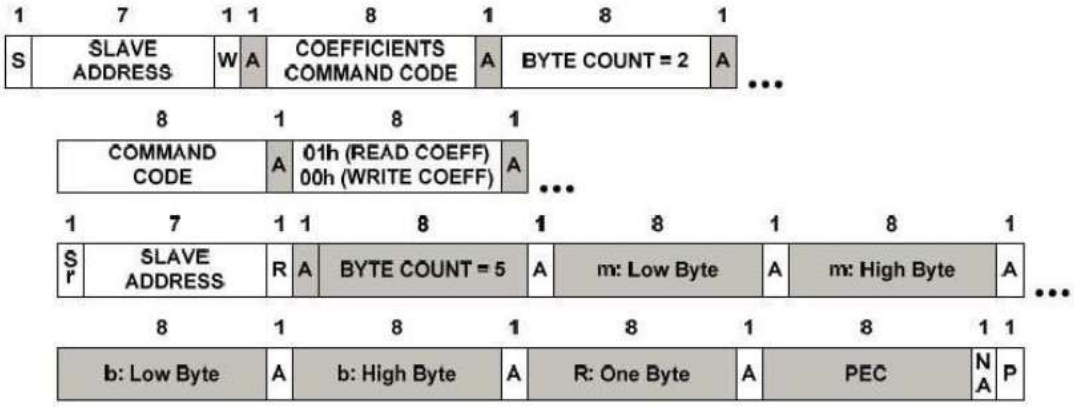


10.12 Coefficient (30h)

The power supply shall support the PMBus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

Command	COEFFICIENTS support	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

Figure 10.6. Retrieving Coefficients Using PEC



10.13 Fan_config_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the PMBus device whether or not a fan associated with position 1(or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the PMBus device the number of tachometer pulses per revolution each fan provides. This information is needed to commanding and reporting fan speed in RPM. Two bits are provided for each fan.

These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

00b = 1 pulse per revolution,

01b = 2 pulses per revolution,

10b = 3 pulses per revolution,

11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

Table 10.6. FAN_CONFIG_1_2 Command

Bits	Value	Meaning
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	0	No fan in position 2
2	Not used	
1:0	Not used	

10.14 Fan_command_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is RPM.

10.15 Read_fan_speed_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the PMBus linear format.

10.16 PMBus_revision (98h)

This is a correction to the table in the PMBus part II specification regarding the PMBUS_REVISION command.

Table 10.7. PMBUS_REVISION Command

Bits [7:4]	Part I revision	Bits [3:0]	Part II Revision
0000	1.0	0000	1.0
00001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

10.17 Mfr-efficiency _LL(AAh)

The MFR_EFFICIENCY_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the PMBus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

Table 10.8. MFR_EFFICIENCY_LL

Byte Number	Byte Order	Description
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	

2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.

10.18 Mfr-efficiency _HL(ABh)

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the PMBus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

Table 10.9. MFR_EFFICIENCY_HL

Byte Number	Byte Order	Description
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	

6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.

10.19 Read Ein(86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 10.10. READ_EIN Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b =00h		PMBus data format; refer to PMBus specification for details.
P sample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate P sample.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while Testing accuracy.
IMPORTANT: The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).			

10.20 Read Eout(87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 10.11.READ_EOUT Requirements Summary

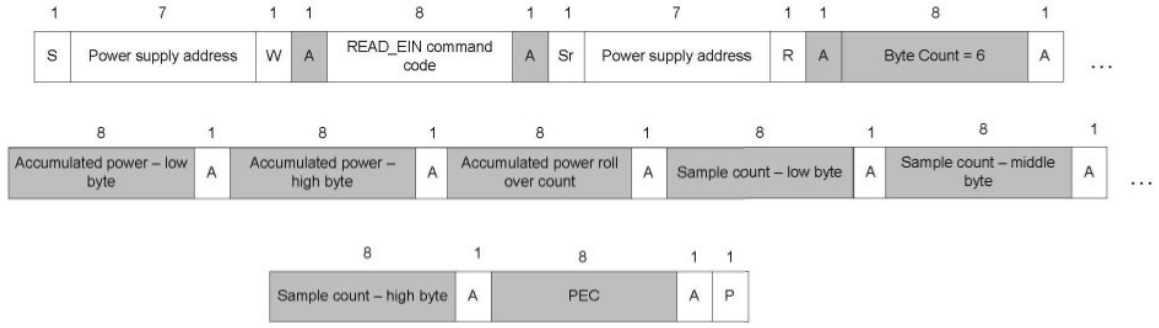
	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b =00h		PMBus data format; refer to PMBus specification for details.
Psample averaging period	Nominal 50msec		Period instantaneous input power is averaged over to calculate P sample.
Sampling period	Nominal 50msec		Period at which the power accumulator and sample counter are updated
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

10.21 READ_EIN & READ_EOUT Formats

The READ_EIN and READ_EOUT commands shall use the PMBus direct format to report an accumulated power value and the sample count. The PMBus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

Figure 10.7. READ_EIN Command

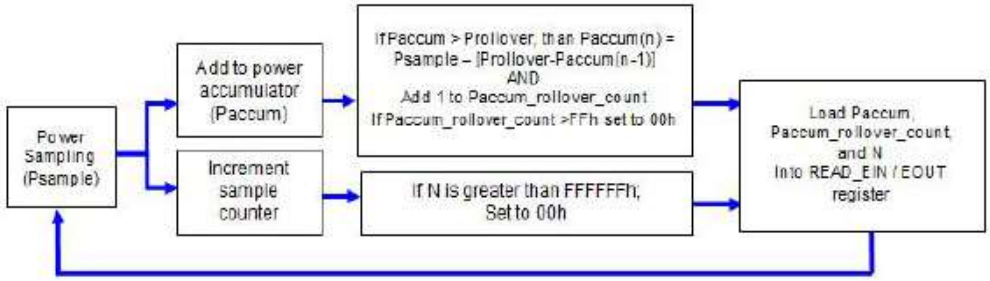


The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_ EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the

roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

Figure 10.8. READ_EIN PSU Functional Diagram



P sample:	The sampled power value in linear or direct format
Paccum:	2 bytes in PMBus linear or direct format. The accumulated power values made up of P sample(0) + P sample(1) + ⋯ + P sample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
P rollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

10.22 Power Supply Accuracy

The following PMBus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC; DC input: 220Vdc -260Vdc); maximum deviation for the ambient temperature is +/- 4°C.

Table 10.12: Power PMBus Accuracy

	Pin<100W	Pin>100W	
Pin	±10W	±5%	
	Iin: 0.25~1.6A	**Iin: >1.6A**	
Iin	**±0.08A or**±5%	±5%	
	10%-20% of Max. Load	**20%~50% of Max. Load**	**50%~100% of Max. Load**
Iout	±5% or ±1A	±3%	±3%
Pout	±5% or ±10W	±3%	±2%
	0%~20% of Max. Load	**20%~50% of Max. Load**	**50%~100% of Max. Load**
Vout	±3%	±3%	±3%
Vin	±5%	±5%	±5%

Preferred data format is the “Linear Data Format” as specified by PMBus specification Part II version 1.2.

10.23 Linear Data format

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

Output Current,

Input Voltage,

Input Current,

Operating Temperatures,

Time (durations), and Energy Storage Capacitor Voltage.

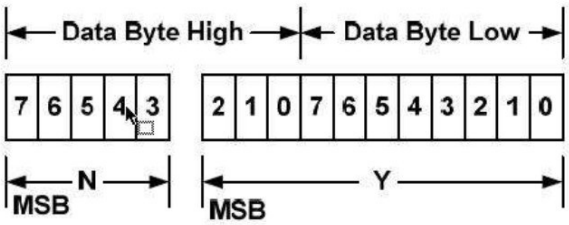
The Linear Data Format is a two byte value with:

An 11 bit, two's complement mantissa and,

A 5 bit, two’ s complement exponent (scaling factor),

The format of the two data bytes is illustrated in Figure 5.1 as show below.

Figure 10.9. Linear Data Format Data Bytes



The relation between Y, N and the "real world" value is:

X = Y·2N

Where, as described above:

X is the "real world" value;

Y is an 11 bit, two' s complement integer; and

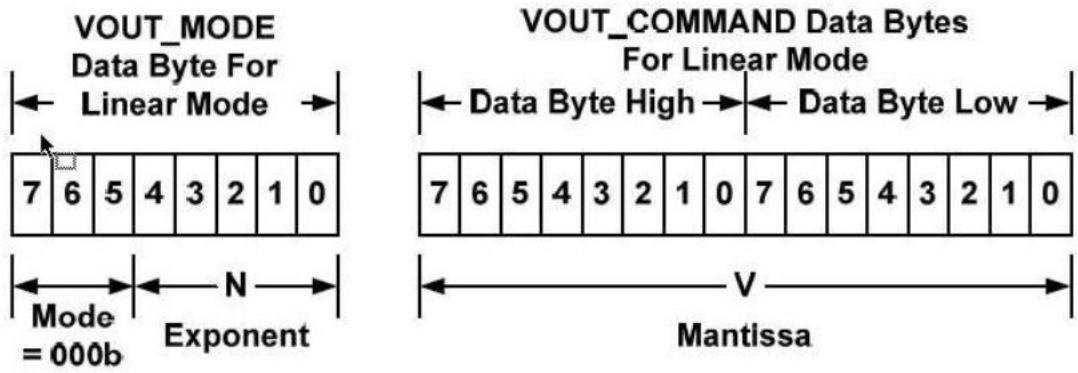
N is a 5 bit, two' s complement integer.

Devices that use the linear format must accept and be able to process any value of N.

10.24 Vout_Mode(20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit exponent. The three bit Mode shall be set to indicate the LINEAR mode for output voltage related commands.The five bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

Figure 10.10. Linear Format Data Bytes



The voltage, in volts, is calculated from the equation Voltage = V·2N, where:

V is a 16 bit unsigned binary integer

N is a 5 bit two's complement binary integer

Sending the VOUT_MODE command with the address set for writing is not supported. If the system sends a VOUT_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS_CML register

11 Cold redundancy

11.1 Overview

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies; including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant roll (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shut down or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.

Figure 11.1. Cold Redundancy 1+1 Functional Block Diagram

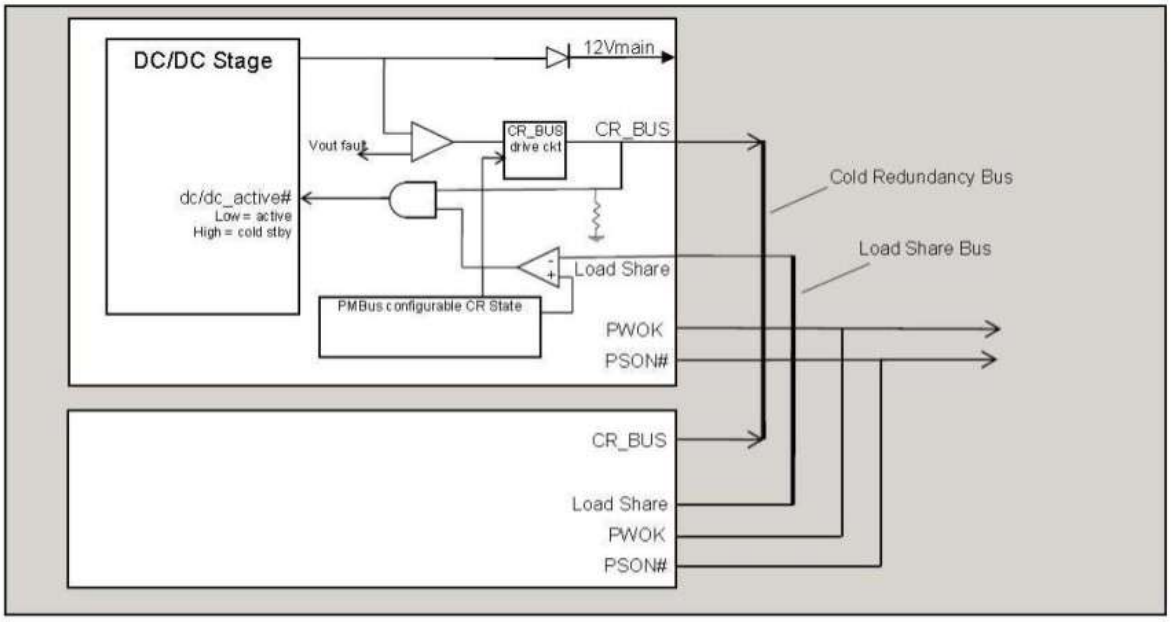


Table 11.1. Logic Matrix for Cold Standby Power Supplies

CR_BUS	Load Share	dc/dc_active#	Cold Standby Power Supply State(s)
High	< VCR_ON	High	Cold Standby
Low	< VCR_ON	Low	Active
High	> VCR_ON	Low	Active
Low	> VCR_ON	Low	Active

11.2 Powering on Cold Standby supplies to maintain best efficiency

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at.

Table 11.2. Example Load Share Threshold for Activating Supplies

	Enable Threshold for VCR_ON_EN	Disable Threshold for VCR_ON_DIS	CR_BUS De-asserted / Asserted
Standard Redundancy	N/A; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2V (40% of max)	90% x (3.2V x 1/2) = 1.44V	OK = Tri-state Fault = Low
Cold Standby 2 (03h)	5.0V (62% of max)	90% x (5.0V x 2/3) = 3.01V	OK = Tri-state Fault = Low
Cold Standby 3 (04h)	6.7V (84% of max)	90% x (6.7V x 3/4) = 4.52V	OK = Tri-state Fault = Low

Notes:

Maximum load share voltage = 8.0V at 100% of rated output power

These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

11.3 Powering on Cold Standby supplies during a fault or over current condition

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100µsec.

11.4 Cold Redundancy PMBus Commands

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. We will call the command Cold_Red undancy_Config (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

Table 11.3. Cold_Redundancy_Config (D0h)

Value	State	Description
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1 [1]	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2 [1]	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3 [1]	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.

1 When the CR_BUS transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (Cold_redundancy_Config = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the Cold_Redundancy_Config command.

11.5 Cold Redundant Signals

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies; the CR_BUS.

12 Blackbox

12.1 Black box function description

This specification defines the requirements for power supplies with PMBus capability to store PMBus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown .The data can be accessed via the PMBus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

12.2 When data is saved to the Black Box?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

12.3 Black Box Events

- There are two types of data saved in the black box:
- 1) System Tracking Data.
- 2) Power supply event data.
- System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system

12.4 Black Box Process

- System writes system tracking data to the power supply RAM at power ON.
- System writes the real time clock data to the PSU RAM once every ~5 minutes.
- Power supply tracks number of PSON and AC power cycles in EEPROM.
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM

- Upon a fault event that causes the PSU to shut down all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

12.5 Related command of Black box

The following command set will be used for Black Box function via the Host System. The commands and protocol used by the Host System and shall be implemented by the microcontroller are defined by this document

Command Code	Command Name	SMBus Transaction Type	Number Of Data Bytes	Remark
DCh	MFR_BLACK_BOX	Read only(7)	237	Read the data of the Black box.
DDh	MFR_REAL_TIME	Read/Write(6/7)	4	Read/Write the data of MFR real time.
DEh	MFR_SYSTEM_BLACK _BOX	Read/Write(6/7)	40	Read/Write the data of MFR system black box.
DFh	MFR_BLACKBOX_ CONFIG	Read/Write(2/3)	1	Read/Write the data of MFR black box configure
E0h	MFR_CLEAR_BLACK- BOX	Write only(1)	1	Send one byte to clear all data of black box.

1) **Command Name: MFR_BLACKBOX**

Format: Read Block with PEC (237 bytes)

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Code:DCh

	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This include the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCII characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a black box event occurs the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

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	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These value shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power	Lower ½	
	shutdown on output		
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no Shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	

Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

2) Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSIC.

3) Name: MFR_SYSTEM_BLACK_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

Code: DEh

The system uses this command to write the following data to the PSU.

Item	**Bytes**	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

4) Name: MFR_BLACKBOX_CONFIG

Format: Read/Write Byte with PEC

Code: DFh

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		Reserved

5) Name: MFR_CLEAR_BLACKBOX

Format: Send Byte with PEC

Code: **E0h**

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.

This command is write only. There is no data byte for this command.

12.6 Hardware Requirements

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied and power is only applied at the standby output pins by an external source (12Vstby).

13 Bootloader

13.1 Boot loader function description

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

13.2 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1)Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1) **Boot Loader**: This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

2) **Main Program:** This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

13.3 Power supply operating mode during and after firmware update

1) Firmware update mode in ON state with no power cycle needed:

Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

2) Bad image after firmware update:

The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

13.4 Firmware Image Header

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	G	Model Name 12 bytes
Byte 12	1	
Byte 13	2	
Byte 14	5	
Byte 15	1	
Byte 16	-	
Byte 17	3	
Byte 18	5	
Byte 19	0	
Byte 20		
Byte 21	W	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major	Firmware Revision 3 bytes;
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

13.5 Firmware update process

Figure 13.1. PSU Upload Process

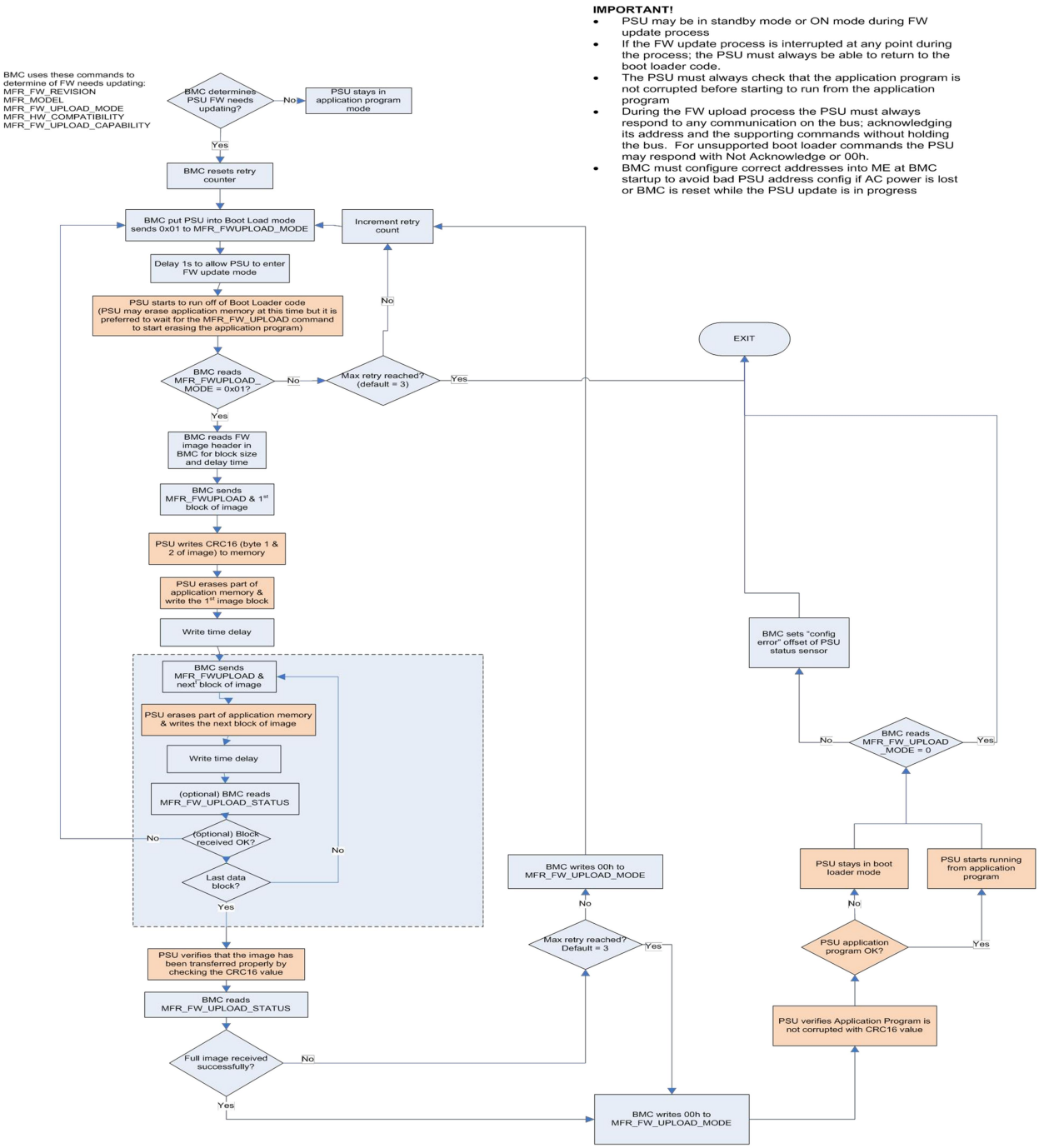
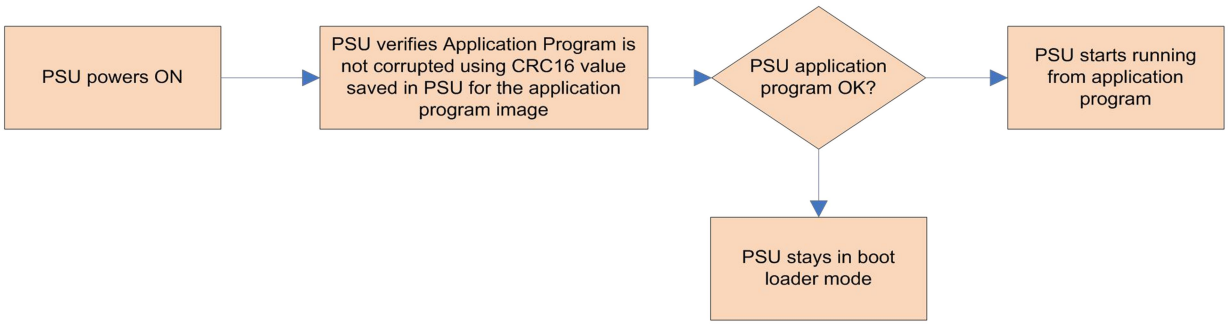


Figure 13.2. PSU flow during powering ON



13.6 Related command of Bootloader

1).Name: MFR_HW_COMPATIBILITY

Format: Read Word
Code: D4h

Bytes	Value	Description
low	ASCII code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCII code for second letter/number of the PSU HW compatibility.	

2).Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte
Code: **D5h**

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Bit	**Value**	**Description**
0(for future use)	1 = PSU support FW uploading in standby mode only	For future use
1(for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

3) **Name: MFR_FWUPLOAD_MODE**

Format: Read/Write Byte

Code: **D6h**

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

4).Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

Bytes	Value	Description
Block size Defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 13.4. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

5).Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: **D8h**

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.

Reset: all bits get reset to '0' when the power supply enters FW upload mode.

Bit	Description
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3(for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.

4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

6).Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: **D9h**

Bytes	Value	Description
0	0-255	Minor revision; secondary
1	0-255	Minor revision; primary
2	0-255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed, but recommended to follow. 0 → No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

7).MFR_MODEL (existing PMBus command)

Code: **9Ah**

Maximum of 12 byte value; ending in terminator character.

8).MFR_REVISION (existing PMBus command)

Code: **9Bh**

14 Reliability / Warranty / Service

14.1 Component de-rating

The following component de-rating guidelines shall be followed. Any exceptions are subject to final approval.

Semiconductor junction temperatures shall not exceed 120℃; (80% of max temperature)

Transformer temperature shall not exceed 110℃& not violate safety' s requirement;

Inductor case temperature shall not exceed 90% of rated temperature in℃.

Capacitor case temperature shall not exceed 90% of rated temperature in ℃.

Resistor wattage de-rating shall be > 20%

Component voltage and current de-rating shall be > 10%

During abnormal conditions (such as a short circuit and the like) no de-rating is required as long as the max rating is not exceeded.

Note: Bulk Cap is an exception to be able to work at maximum rated voltage.

14.2 Life requirement

The power supply shall support 5 year calculated life with a 90% confidence under the following conditions:

100-240VAC input

45℃ inlet temperature

80% of output max-load

14.3 Mean time between failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours at 100% load and 25℃, as calculated by Bell core Telcordia SR-332- Issue 2.

2-250,000 hours demonstrated at 75% load and 40°C.

14.4 Warranty period

Three (3) years.

15 Product regulatory requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations.

The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

15.1 Product safety compliance

UL62368-1/CSA 62368-1 (USA / Canada)

IEC62368-1 (international)

CB Certificate & Report, IEC62368-1 (Report to include all country national deviations)

The following options can be added :

CE - Low Voltage Directive 2014/35/EU (Europe)

GB4943- CNCA Certification (China)

15.2 Product emc compliance – class a compliance

Note: The product is required to comply with Class A emission requirements as the end system that it is configured into is intended for a commercial environment and market place. Power supply is to have minimum of 6dB margin to Class A Limits to support Customer’ s margin requirements. (For conduct EMI, can have a minimum of 6 db margin to class A limits.)

FCC /ICES-003 - Emissions (USA/Canada)

EN55032 – Conducted & Radiated Emissions (Europe)

EN55035 - Immunity (Europe)

EN61000-4-2 Electrostatic Discharge

EN61000-4-3 Radiated susceptibility

EN61000-4-4 Electrical Fast Transients/ burst

EN61000-4-5 Surge

EN61000-4-6 Conducted susceptibility

EN61000-4-8 Power Frequency Magnetic Field

EN61000-4-11 Voltage Dips and Interruption

*EN61000-3-2 – Power Harmonics (Europe)

*EN61000-3-3 – Voltage Fluctuation and Flicker (Europe)

CE – EMC Directive 2014/30/EU (Europe)

VCCI (Japan)

GB 9254 – (EMC) Certification (China)

GB 17625.1 - (Harmonics) CNCA Certification (China)

15.3 Certifications / registrations / declarations

Optional:

cULus/or cTUVus Certification (US/Canada)

CB Certificate & Report

CE Declaration of Conformity (CENELEC Europe)

FCC/ICES-003 Class A Attestation (USA/Canada)

CNCA Certification (China)

BSMI Certification (Taiwan)

Ecology Declaration (International)

KCC-Mark(Korea)--option

Notes:

a.Certification shall be done to the most recent standard editions.

b.To support ALPHA or BETA development power supply shipments, at least one 3rd party Certification is required (e.g. NEMKO, UL, etc.).

c.Power Supply Vendor requires providing copy of each certification.

15.4 Component regulation requirements

A.All Fans shall have the minimum certifications: UL and TUV or VDE

B.All current limiting devices shall have UL and TUV or VDE certifications and shall be suitable rated for the application where the device in its application complies with IEC60950.

C.All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printed wiring board manufacturer.

D.All connectors shall be UL recognized and have a UL flame rating of UL94V-0

E.All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer. SELV Cable to be rated minimum 80V, 130C

F.Product safety label must be printed on UL approved label stock and printer ribbon. Alternatively labels can be purchased from a UL approved label manufacturer.

G.The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

15.5 Product ecology requirements

All materials, parts and subassemblies must not contain restricted materials as defined in Customer's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers –Compliance to Customer's content specification incorporates compliance requirements for the European Union's (EU) Restriction of Hazardous Substances (RoHS).

15.6 Harmonics and voltage flicker compliance information

Input Line Current Harmonic Content (PFC)

The power supply shall meet the requirements of EN61000-3-2 Class Aand the Guidelines for the Suppression of Harmonics in Appliances and General Use Equipment Class A for harmonic line current content at full rated power.

Table Harmonic Limits for Class A equipment

	Per: EN61000-3-2		Per: JEIDA MITI
Harmonic Order	Maximum permissible Harmonic current at 230Vac/50Hz inAmps		Maximum permissible Harmonic current at 100Vac/50Hz inAmps
Odd harmonics			
3	2.3		5.29
5	1.14		2.622
7	0.77		1.771
9	0.4		0.92
11	0.33		0.759
13	0.21		0.483
15≤n ≤39	0.15x (15/n)		0.345x (15/n)
Even harmonics			
2	1.08		2.484
4	0.43		0.989
6	0.3		0.69
8 ≤ n ≤ 40	0.23x (8/n)		0.529x (8/n)

15.7 Other Safety Requirement Notations

15.7.1 Leakage current maximums

Maximum leakage current to ground shall be less than 3.5mA at 264Vac, 63Hz.

15.7.2 Max surface temperatures

The temperature of the power supply chassis shall not exceed 70 ℃ under all circumstances.

Otherwise a UL international HOT SURFACE label is required. If this HOT SURFACE label is required, it shall be placed in such a manner that when the power supply is extracted from the system, the label shall be visible before the operator

has a chance to touch the hot surface of the power supply.

15.7.3 Date coded serial numbers

Power supply shall be marked with a date-coded number for traceability purposes .

15.7.4 Power input electrical ratings

Power supply shall be tested to allow Nominal AC input operating voltages(100-127VAC and 200-240 VAC) and current rating. 127V is required for countries such as Mexico. The earth safety conductor shall be color-coded green/yellow and suitable sized for the max current of the power supply.

15.7.5 Maximum allowable temperatures on inlet receptacles

The inlet receptacle shall be suitably rated for the maximum operating temperature to the power supply, when installed in a rack environment.

15.7.6 Maximum allowable temperatures on power cords

The exhaust air of the power supply shall not impose temperatures that will exceed the maximum allowable temperature of the power cord.

15.7.7 Insulation requirement

All the outputs shall be isolated from the AC input to meet safety agency requirements.

The test shall be applied between primary (AC Line and Neutral) and Earth ground (Input receptacle ground terminal).

Voltage: 1800Vac or 2546Vdc Arcing sense=8

Trip Current Sensitivity: < 10mA. Duration: 1 minute

The power supply module in the system shall be test at 500Vdc, insulation resistance shall be more than 100Mohms.

15.8 Power supply cage & module regulatory & safety markings

The power supply vendor shall mark the power supply with the following product regulation markings. Optional:

15.9 Other safety / regulatory marks on power supplies

15.9.1 Power supply Model Designation

The power supply model designation must be marked on the power supply.

All regulatory certifications and documents must carry the same model designation for traceability purposes.

15.9.2 Electrical input&output ratings

The AC or DC electrical input ratings (V, A, Hz), and secondary electrical output ratings (V, A, W >total output power<) must be marked on the power supply. If possible, the end system input electrical ratings should also be marked on the power supply. These markings need to be visible to the outside of the end system. These electrical rating for the end system may be different than the ones for the power supply – this is acceptable. Marking the power supply with the end system electrical ratings, provides flexibility if the end system may be configured with various power supplies. This ultimately reduces the need to change the end system electrical rating label each time the system is configured with a

different power supply.

15.9.3 AC inlet label&proper earth ground warning

For compliance to EMKO-TSE (74-SEC) 207/94, Clauses 1.7.2, a label with the following verbiage is required as shown below. The label may vary is size and/or shape, however the verbiage must be the same.

Example 1

The proper grounding verbiage may be joined combined with the electrical rating to reduce number of labels used.

15.9.4 Shock hazard&service only warning

The power supply module shall be marked with the international label shown below to indicate that no user serviceable parts are contained in the power supply. This label shall be printed on bright yellow vinyl label stock with black symbols.

Example Only

Size may vary depending on room and location on power supply

15.9.5 Caution hot surface warning

The power supply shall be marked with a Caution Hot Surface Warning label. The labelshall be located in such that when servicing takes place the service person will first see the label.

For redundant type modules, the label should be seen first as the module is being extracted from the power supply cage.

15.9.6 Protective earth ground symbol

The IEC 417, No 5091a protective earth symbol, shall be marked adjacent to the protective earth termination.

15.9.7 Line&neutral terminal markings

The Line and Neutral Terminals coming into the power supply shall be marked with the “L” for Line and “N” for Neutral. Typically these markings are silk screened on the power supply printed wiring board adjacent to the Line and Neutral terminals.

15.9.8 Neutral line fusing

With the use of a fuse in the neutral line, safety requirements (IEC60950, Clause 2.7.6) mandate the following marking must be provided on the equipment.

CAUTION DOUBLE POLE / NEUTRAL FUSING

15.9.9 Fuse markings

The AC fuse (line and/or neutral) shall be marked with the fuse electrical rating and type adjacent to the fuse(s). Also the fuse component designation shall be marked adjacent to the fuse.

Example: F1, 250V, 3A, SB.

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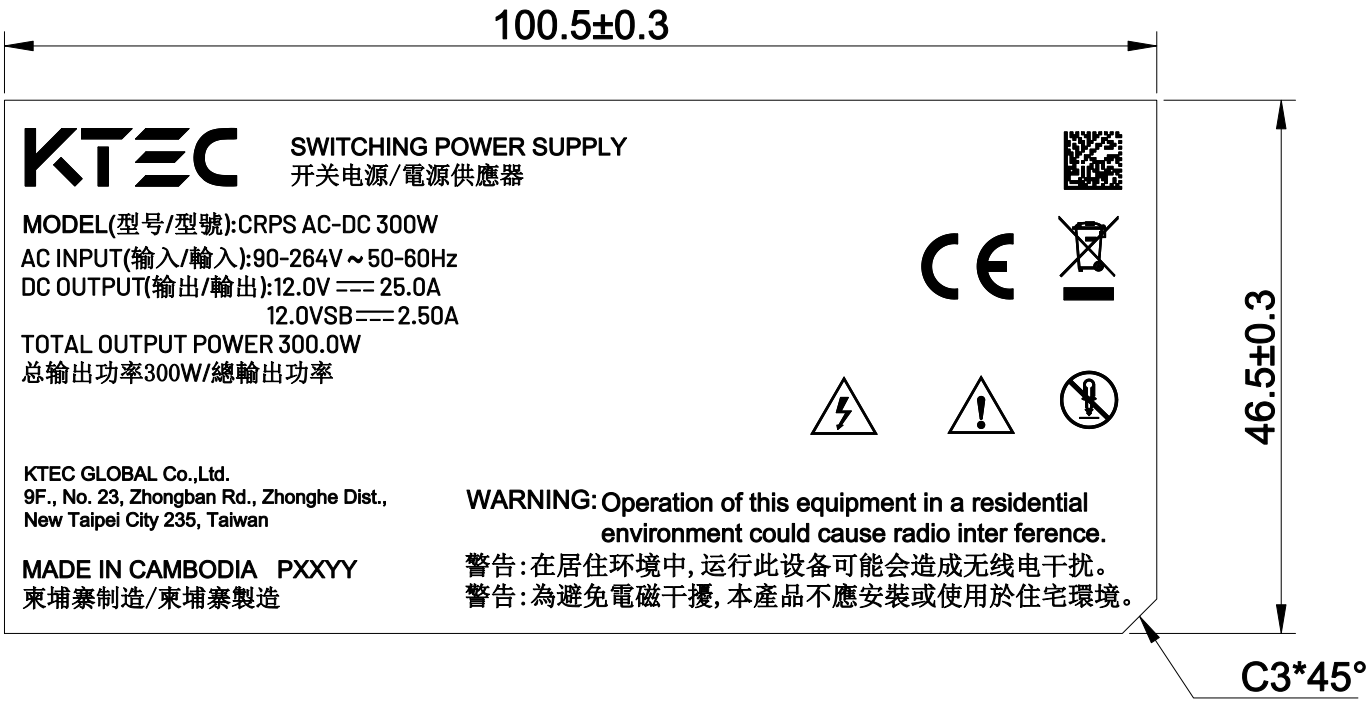
16 Name plate



Note: MATERIAL: silver polyester (消银龙); Thickness: 0.08+-0.01mm

Black characters silver background

PAHS REACH ROHS

PXXYY (P=PAHS, 6P, NP XX=Week, YY=Year), use the actual production date.

SN (Data Matrix Code size: 5*5mm):

First code G(Ktec)＋Production part number (Product code)＋Ten yards of flow code SSSSSSSSSS (decimal)

Total 19 codes

Example： GKE2600180000000001, GKE2600180000000002...GKE2600189999999999.

17 Packing (unit: mm)

TBD